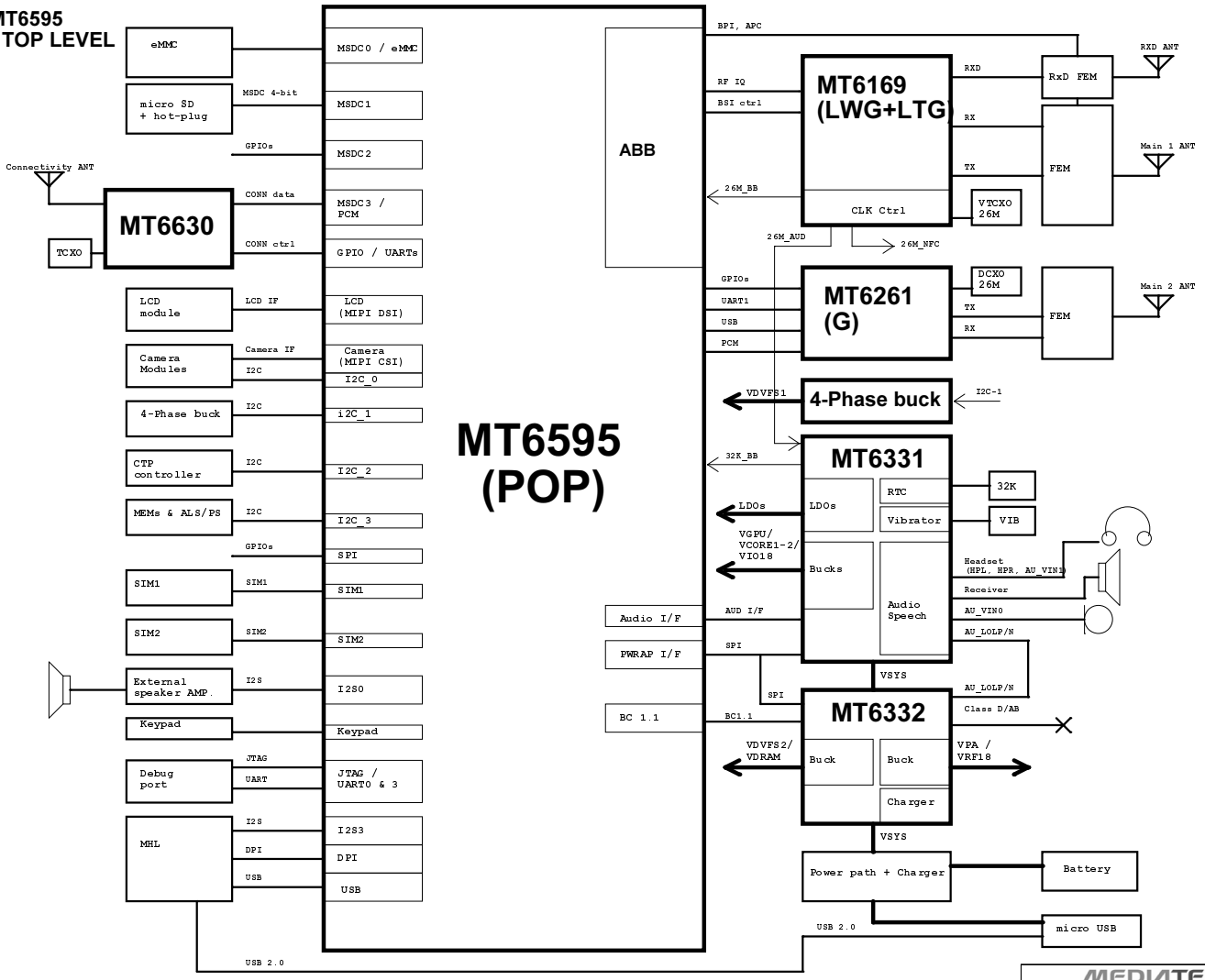
Project : MT6595
REF_SCH TOP LEVEL



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File: 01_Block Diagram

Size: C — Mediatek Confidential

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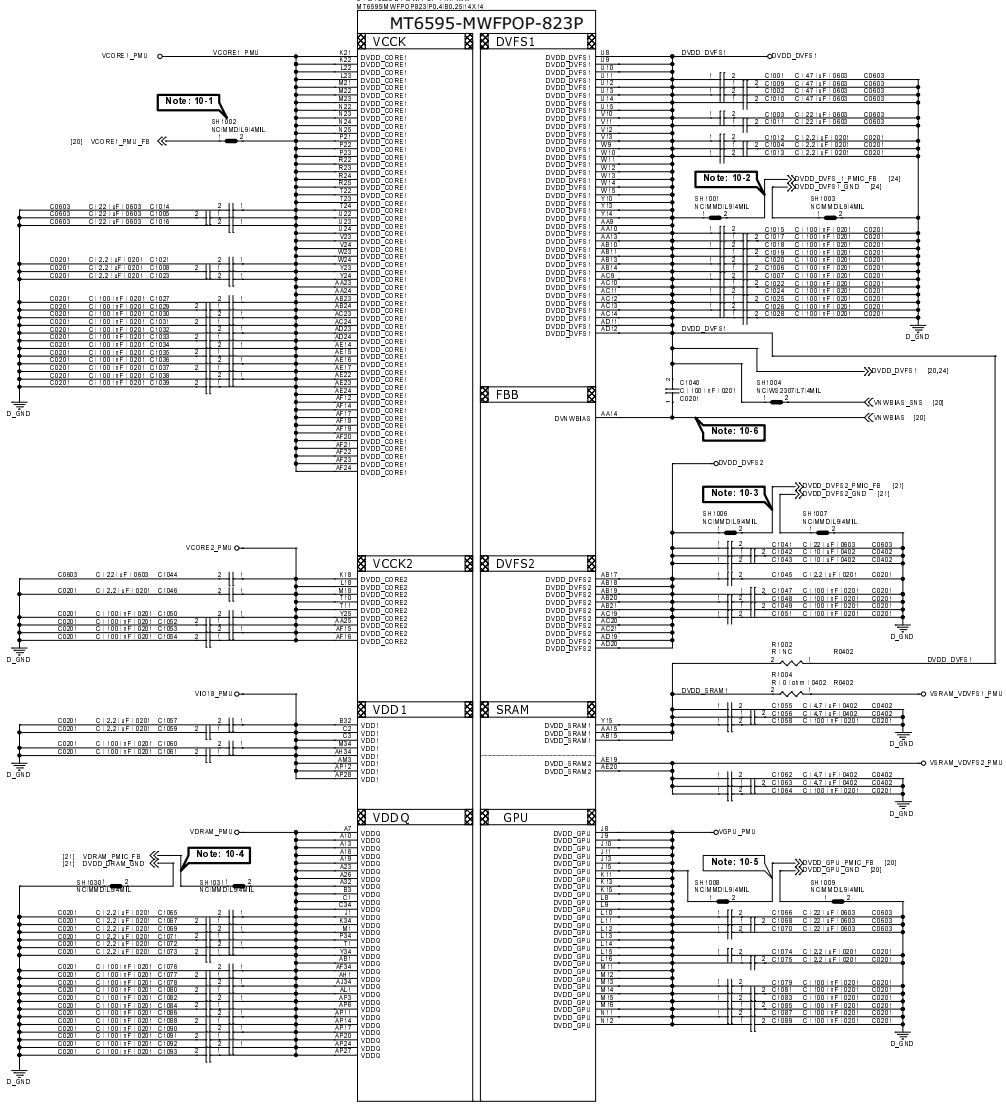
I2C	Function	I2C Spec.	Budgeted Timing	I2C Slave Address (7-bit mode)
I2C-0	Rear Camera	400 Kbps	Yes.	Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (DW9714A) I2C address: 0X18 (Write:0x30, Read:0x31)
	Front Camera	400 Kbps	Yes.	Front camera (OV5648) I2C address: 0X36 (Write:0x6C, Read:0x6D) AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-1	4-Phase buck	3.4 Mbps	Yes.	DA9210 / 4-Phase Buck I2C address: 0X68 (Write:0xD0, Read:0xD1)
	VBAT Boost	3.4 Mbps		TPS61280 / Boost buck I2C address: 0X75 (Write:0xEA, Read:0xEB)
I2C-2	CTP	400 Kbps	Yes.	GT917S / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB)
	SW CHG / PP	400 Kbps		BQ24160YFF / SW CHG + PP I2C address: 0X6B (Write:0xD6, Read:0xD7)
	Flash LED	400 Kbps		LM3642 / Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)
	LCM Gate Driver	400 Kbps		TPS65132AYFFR / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
I2C-3	M Sensor	400 Kbps		AK8963C / M-Sensor I2C Address: 0x0C (Write:0x18, Read:0x19)
	A+Gyro Sensor	400 Kbps	Yes.	MPU-6050C / A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Baro Sensor	400 Kbps		BMP180 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	RGB / PS Sensor	400 Kbps		CM36652 / RGB+PS I2C address: 0X60 (Write:0xC0, Read:0xC1)
	NFC	1.2 Mbps	Yes.	NFC I2C address: 0X28 (Write:0x50, Read:0x51)
	Speaker AMP.	400 Kbps		TFA9887 / Speaker AMP I2C Address: 0x36 (Write:0x6C, Read:0x6D).
	MHL	400 Kbps		MHL I2C Address = 0x3B/3F/4F. (Write:0x76/7E/9E, Read:0x77/7F/9F if CI2CA = High.) MHL I2C Address = 0x39/3D/4D. (Write:0x72/7A/9A, Read:0x73/7B/9B if CI2CA = Low.)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Date	Category	Item	SW Modification
2014.01.28	General	0.01 Pre-release	
2014.02.13	BB	1. 95 PCM connect to MT6261, DAI connect to MT6630	
2014.02.14	RF	1. B34/39 use DPDT for co TRX filter, to save SP16T port 2. Change all the DP4T to RF1624 3. MT6261 G900 RX SAW change to "SAFFB942MAN0F0A"	
2014.02.17	CTP	1. Delete R6103.	
2014.02.17	USB	1. correct U2420, U2420 part number	
2014.02.24	BB	1. Change all 0402 PDN capacitors to 0201. 2. Delete R1301/R1302. Connect USB_VBUS_P0 (C8 ball) pin to GND. since USB OTG "B-Valid" detection has implemented by MT6332's ADC. 3. Connect VCC18IO_CMR (E26 ball) to "VIO18_PMU" since I2C-2 I/O power is powered by VCC18IO_CMR. 4. Optimize BB I/O de-coupling capacitors in "11_BB_POWER_2" page. 5. Re-map MT6595 GPIO in "13_BB_2" page: 5.1 EINT9 => "2GMD_EXP_INTB"; EINT2 =>"2GMD_WDT_INTB" to support FIQ. 5.2 EINT14 = > "SUB-CAMERA-RESET"; EINT15 => "SUB-CAMERA-PWDN". 5.3 Modify URTS0/UCTS0 GPIO usage for USB SW control. 5.4 Re-arrange Keypad, I2S0 & I2S3 GPIO according to signal fan-out. 6. Update design in "20_POWER_MT6331" page: 6.1. Delete C2016/C2008 NC Cap. 6.2. Delete "AU_LORP" and "USB_B_VALID" net. 6.3. Change net name "VCORE_PDN_PMU" => "VCORE1_PMU". 6.4. Change net name "VCORE_AO_PMU" =>"VCORE2_PMU". 7. Update design in "21_POWER_MT6332" page: 7.1. Modify U2102 control: U2102's VSEL = VSYS; U2102's EN & nBYP = VIO18. 7.2. Merge VDDQ net into VDRAM_PMU. 7.3. Delete ESD2101/ESD2102. 7.4. Use MT6331 VGP2 as backup VM power; Add R2108/NC to fulfill DRAM 1.2/1.8V power sequence. 8. U2401's G1 pin have to driven by MT6595 AO-GPIO. Use MT6595's GPIO103 to instead of "BUCK_CTRL". 9. Modify design in "50_CONNECTIVITY_MT6630" page: 9.1. Delete R5020/R5023/R5025. 9.2. Renew TSX. 9.3. Delete C5053 / Waive analog FM. 10. Modify design in "64_PERI_USB_MHL" page: 10.1. Add U6402 (1.2V LDO) to instead of "VGP2_PMU". 11. Modify DSDA interface: 11.1. Add Q7002. 11.2. Update USB switches control: GPIO115 =>U7005.10; GPIO116 => U7003.10. 11.3. Add L7001/L7002. 11.4. Change U7003/U7005.9 from VSYS to VUSB33_PMU to reduce leakage current. 11.5. Change U6702-3 to U7101-3 to deal with netlist error.	
2014.02.24	CONNECTIVITY	1. Modify design in "50_CONNECTIVITY_MT6630" page: 1.1. Delete TSX. 1.2. Change U5005 part # to "BAL / LDM182G4505EC015 ".	
2014.02.25	BB / RF BPI	1. Modify design in "70_DSDA_Interface" page: 1.1. Replace "LTE_BPI_OUT4" with "LTE_BPI_OUT9". 1.2. Add "LTE_BPI_OUT8" net for 2G USB wake up host.	
2014.02.25	RF ANT	1. Integrate antenna tuner circuit ("ASM_Main2_704~2170MHz") into "36_RF_AT" page.	

Date	Category	Item	SW Modification
2014.02.26	Audio	1. Modify design in "60_PERI_AUDIO_IO" page: 1.1. Main microphone and speaker circuit has been integrated. 1.2 Add R6004/R6005, C6029/C6031 to form low-pass-filter in headphone output.	
2014.02.26	BB	1. Modify design in "70_DSDA_Interface" page: 1.1. Add "LTE_BPI_OUT7" net for 2G memory dump and MD log. 1.2. Add SIM1/2 hot swap detection. 1.3. Add U7006 level shift.	
2014.02.26	RF	Update CSFB DSDA: 1. 3 bypass cap on VCC2 of SKY7778 2. R3224 should be put after VCC Cap 3. 885049 need pi-network matching for 2nd harmonic rejection 4. B38 can't use B41 TX filter 5. bypass cap on VCC2 of SKY7721 6. HPF for G8 Tx in G7 Rx band noise rejection 7. LPF for harmonic rejection 8. B5 LPF is optinal for WIFI band rejection 9. Change U506 ASM SP16T RF1500 to ASM SP12T SKY13488, add a SP5T U1631 for HB Port (SP16T HB loss is a high risk to TDD-LTE HB). 10. Band change to CMCC~s 5家12?ま? ?狠 : remove B8/B20 duplexer U514/U513 , DP4T U3305 U3415 and DRX SAW U3414/U3413 , add EGSM single SAW U3317 11. DRX Switch U3402 change from SP12T RF1662 to SP10T ASM / CXM3633ER, due to remove B8/B20 DRX SAW. 12. B34/39 change from TRX filter re-use to TX and RX filter, to improve TRX linkbudget. Remove DPDT U3206 and B34/39 TX SAW U1617/U1622, add B9916 U502 B34/39 RX Diplexer SAW and AG90A U503 B34/39 TX SAW. 13. Remove MT6169 32K/XO 0ohm R3109, R3111,R3106,R3112. ROME just support VTCXO and no 32Kless 14. Add Car kit CON3304 at MT6261. 15.Add C3218/C3219. MT6169 TX Ouput need a DC block(MUST).	



Schematic design notice of "10_BB_POWER_1" page.

Note 10-1: VCORE_1 remote sense must be close to MT6595's P21 ball.

Remote sense trace with GNDshielding to PMIC (Differential)

Note 10-2: Differential pair of DVFS1 remote sense must be close to MT6595's Y14 ball.

Note 10-3: Differential pair of DVFS2 remote sense must be close to MT6595's AB17 ball.

Note 10-4: VDRAM remote sense must be close to MT6595's A32 ball.

Note 10-5: Differential pair of GPU remote sense must be close to MT6595's J15 ball.

Note 10-6: For VNWBIAS(VFBB), the trace width of VNWBIAS must be >=20mil and its routing length must be as short as possible.

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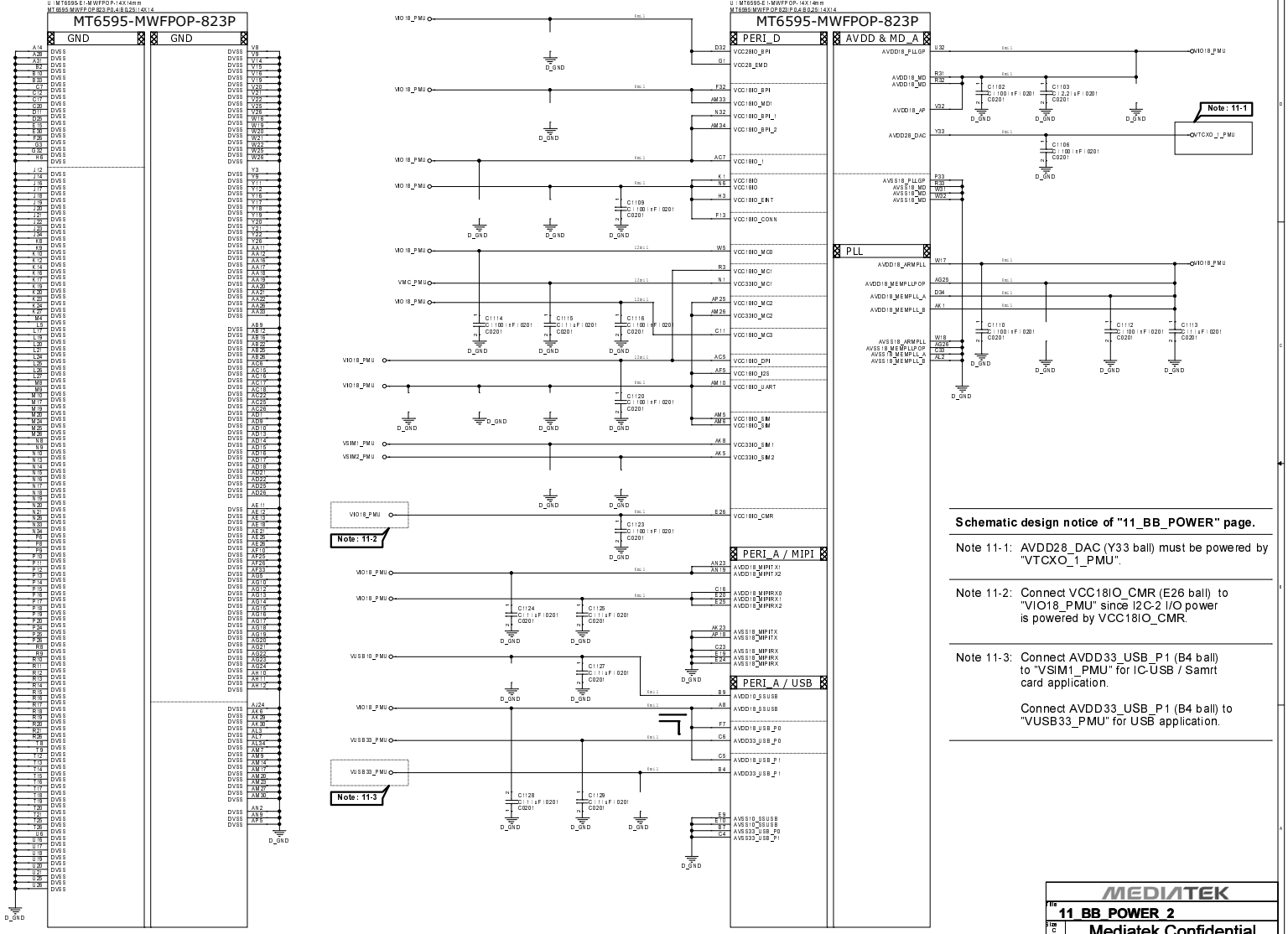

Schematic design notice of "11_BB_POWER" page.

Note 11-1: AVDD28_DAC (Y33 ball) must be powered by "VTCXO_1_PMU".

Note 11-2: Connect VCC18IO_CMR (E26 ball) to "VIO18_PMU" since I2C-2 I/O power is powered by VCC18IO_CMR.

Note 11-3: Connect AVDD33_USB_P1 (B4 ball) to "VSIM1_PMU" for IC-USB / Samrt card application.

Connect AVDD33_USB_P1 (B4 ball) to "VUSB33_PMU" for USB application.

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File: 11_BB_POWER_2

Size: C

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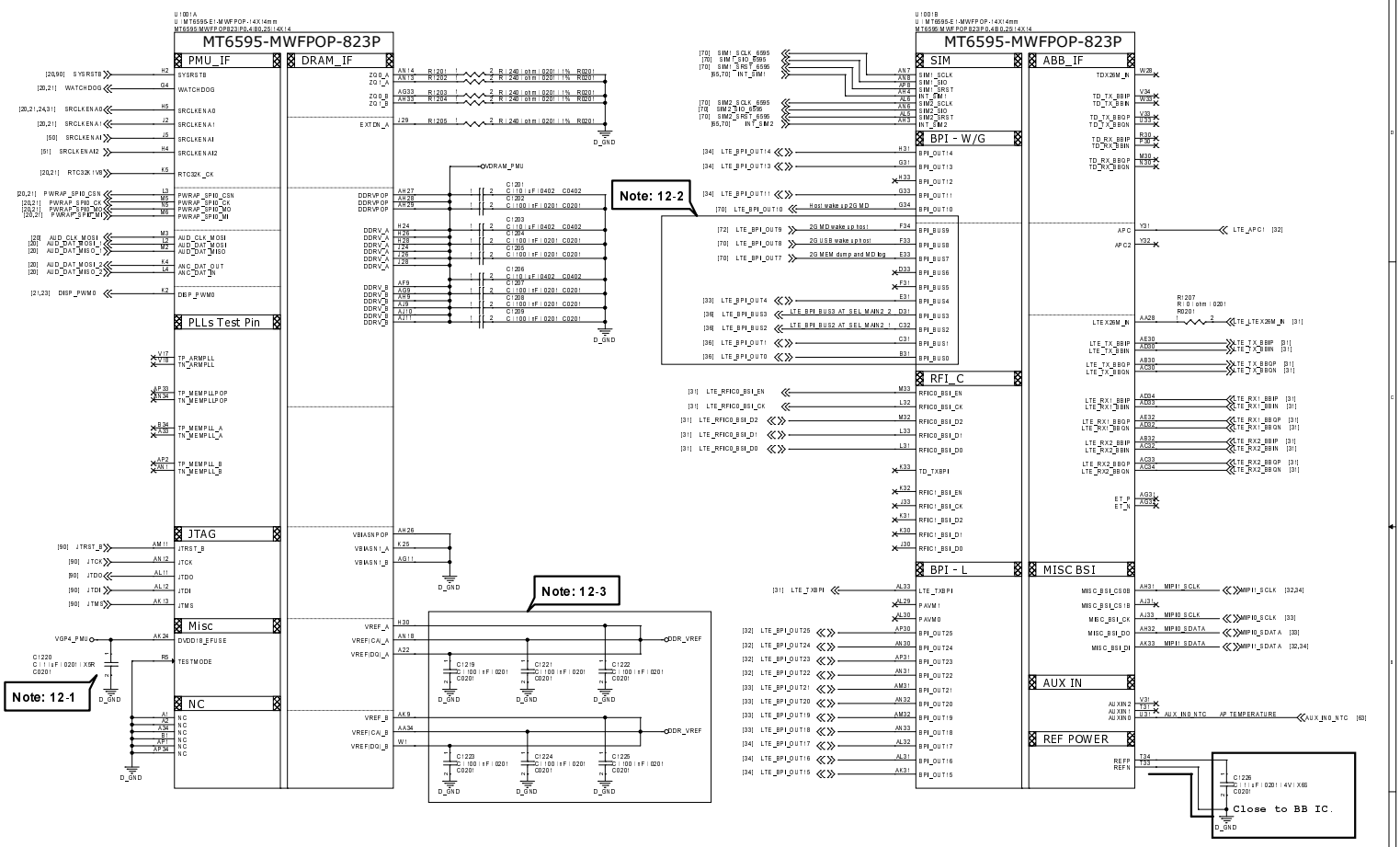

Schematic design notice of "11_BB_11" page.

Note 12-1: Apply 1.8V to DVDD18_EFUSE (AK24) for eFuse programming.

Note 12-2: The BPI_BUS0~BPI_BUS9 are capable of 2.8V I/O operation.

Note 12-3: The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible.

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File: 12_BB_1

Size: C

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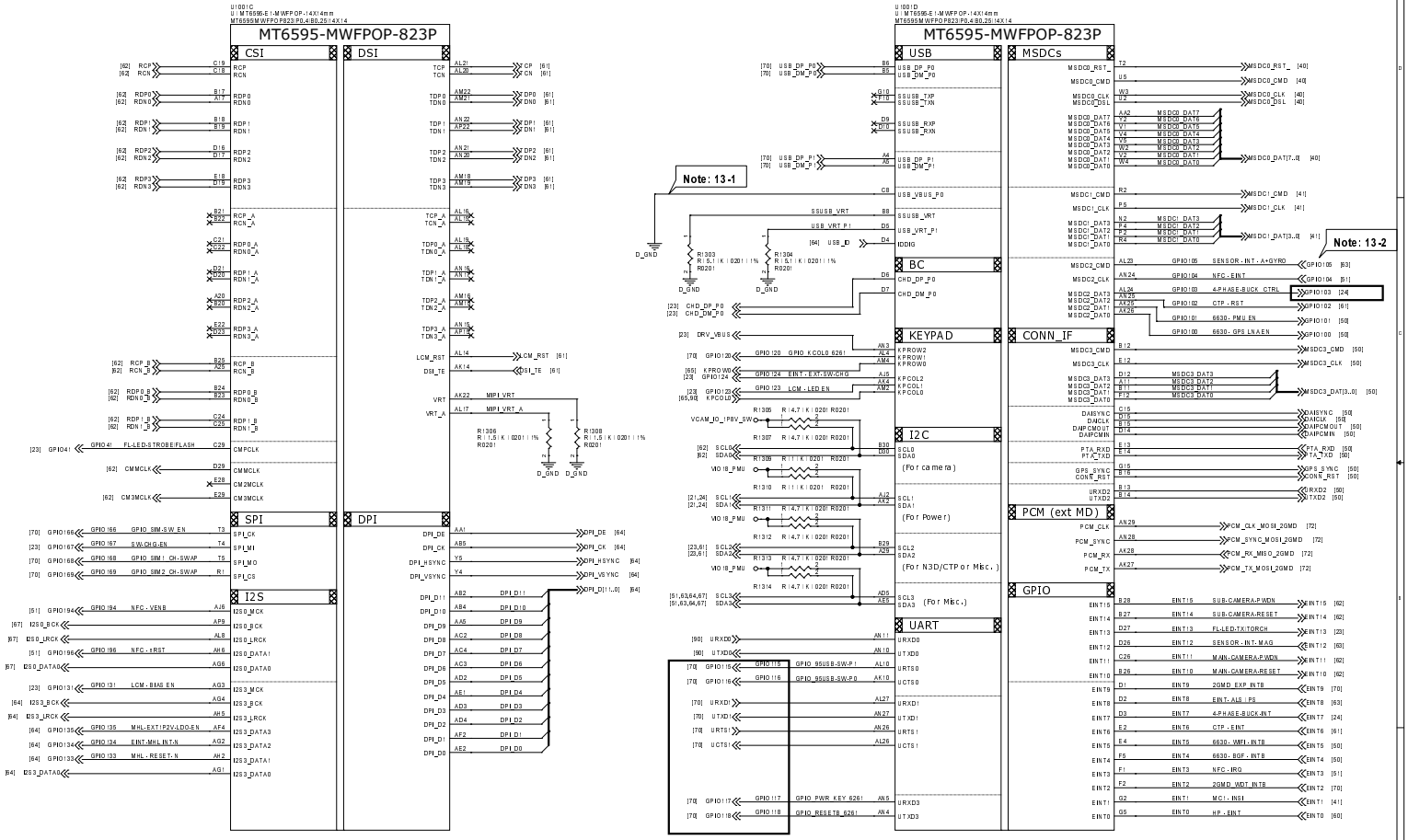

Schematic design notice of "12_BB_2" page.

Note 13-1: Connect USB_VBUS_P0 (C8 ball) pin to GND since USB OTG "B-Valid" detection has implemented by MT6332's ADC.

Note 13-2: GPIO103 is dedicated for DA9210 4-phase buck control.

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File: 13_BB_2

Size: C

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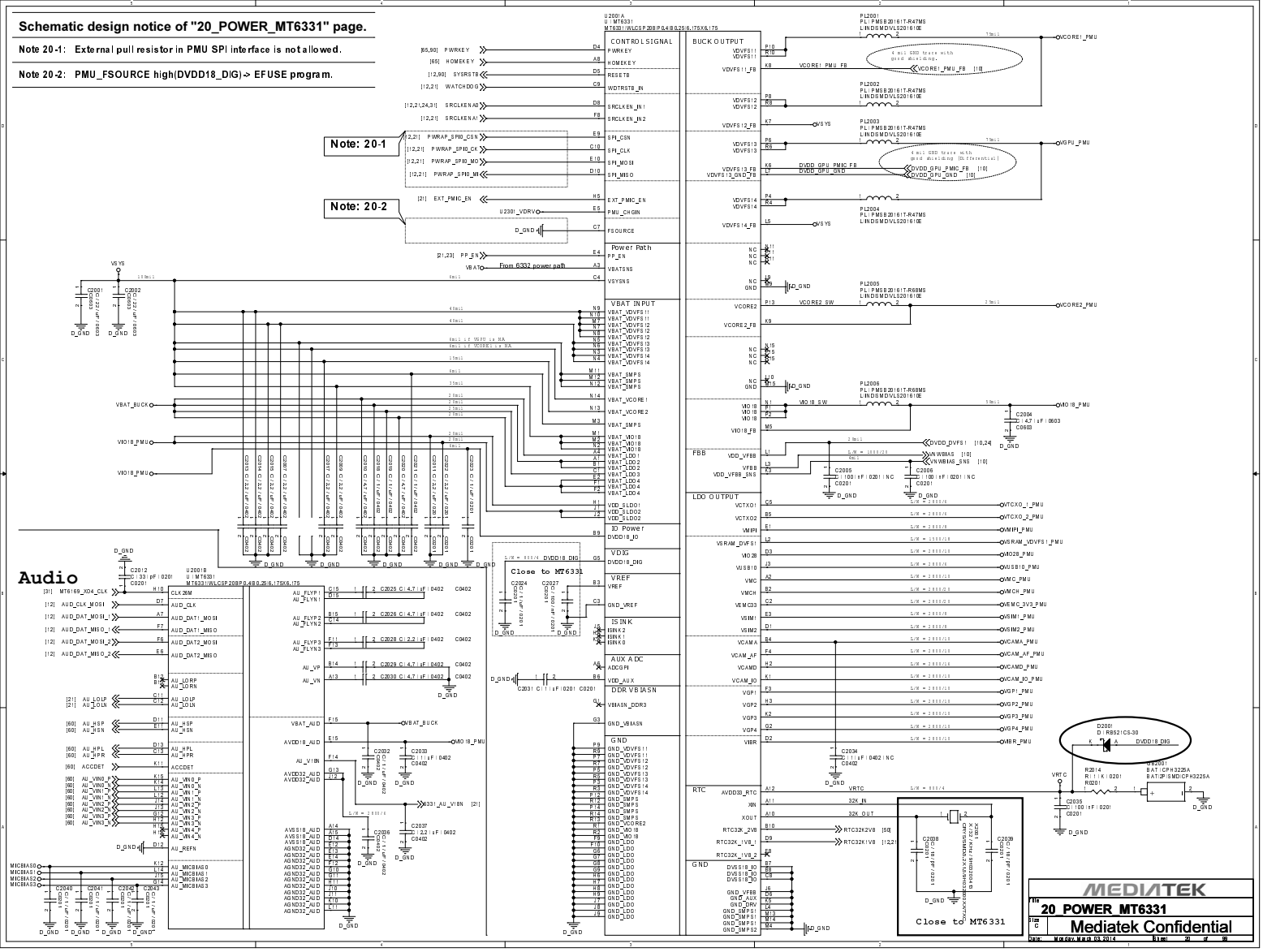
Schematic design notice of "20_POWER_MT6331" page.

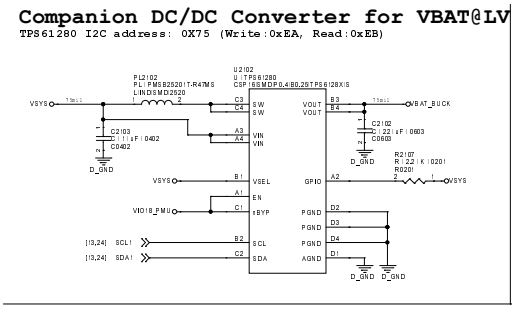
Note 20-1: External pull resistor in PMU SPI interface is not allowed.

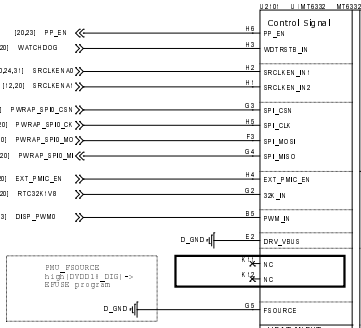
Note 20-2: PMU_FSOURCE high(DVDD18_DIG)-> EFUSE program.

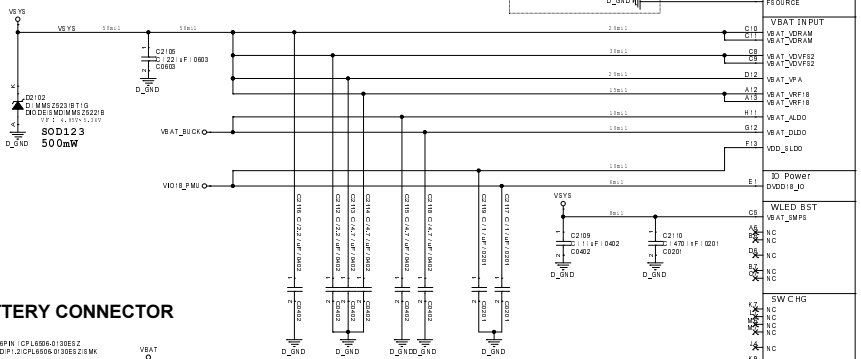


Companion DC/DC Converter for VBAT@LV

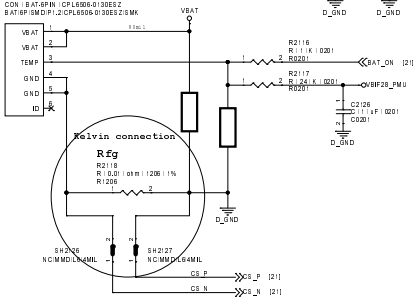
TPS61280 I2C address: 0X75 (Write:0xEA, Read:0xEB)

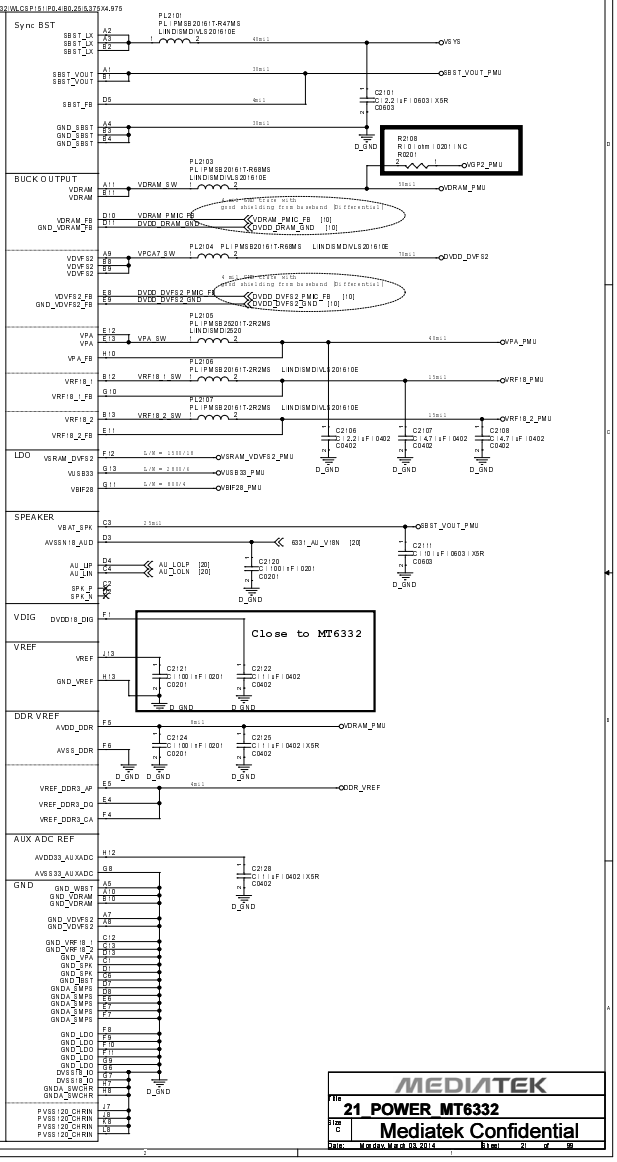






BATTERY CONNECTOR





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File: 22_POWER_WPC_MT3188

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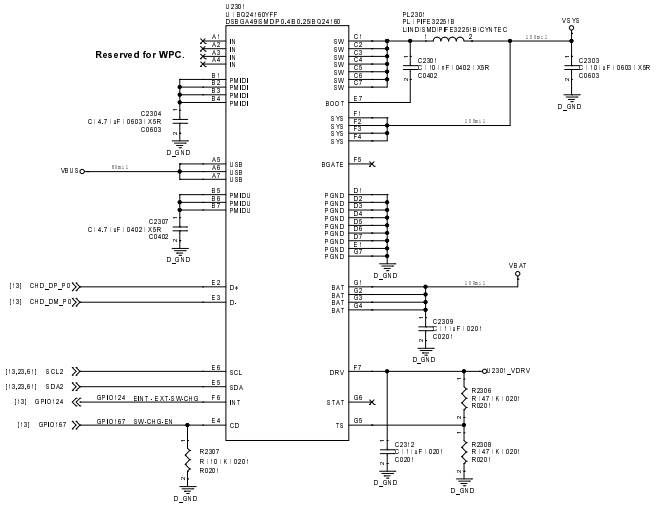
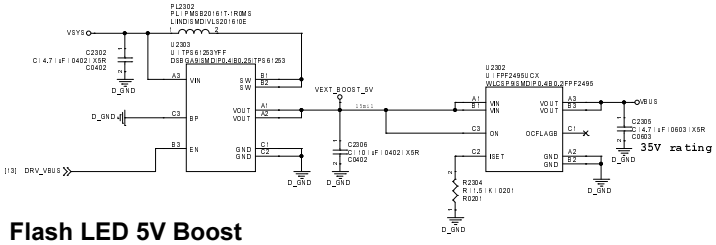
Switching Charger + Power Path

SW CHG + PP I2C address: 0X6B (Write:0xD6, Read:0xD7)
Only support USB and standard charger.

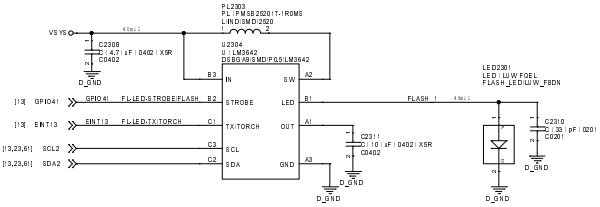


USB OTG 5V Boost

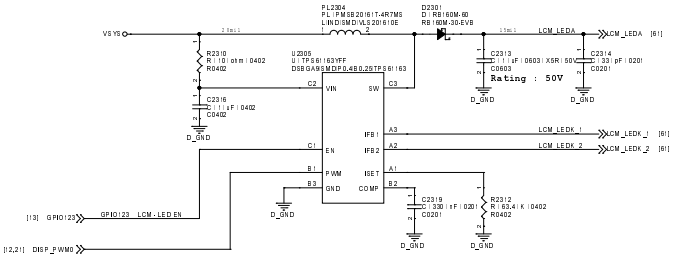


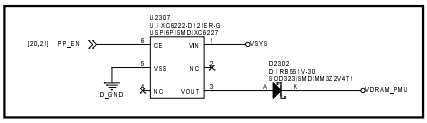
Flash LED 5V Boost

Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)



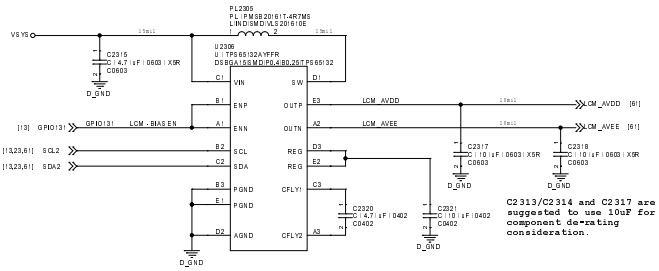
LCM Backlight LED Driver





LCM Gate Drive

LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)



C2313/C2314 and C2317 are suggested to use 10uF for component derating consideration.

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File	23_POWER_THIRD-PARTY
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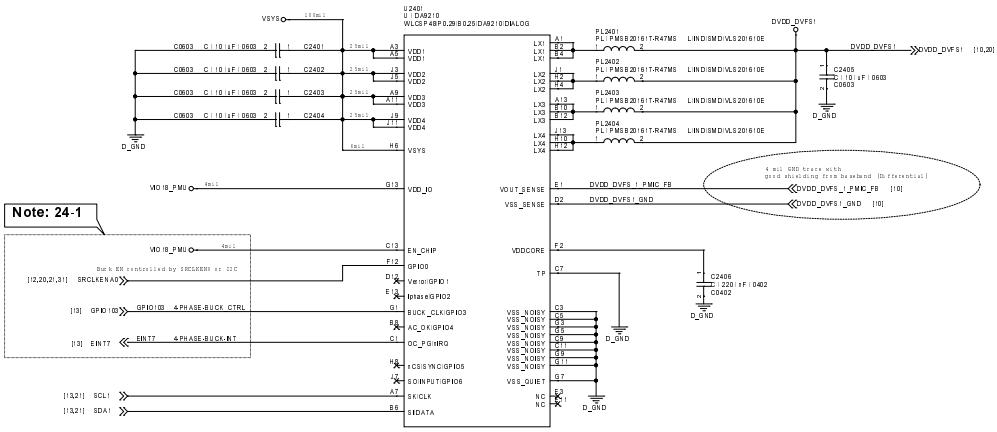
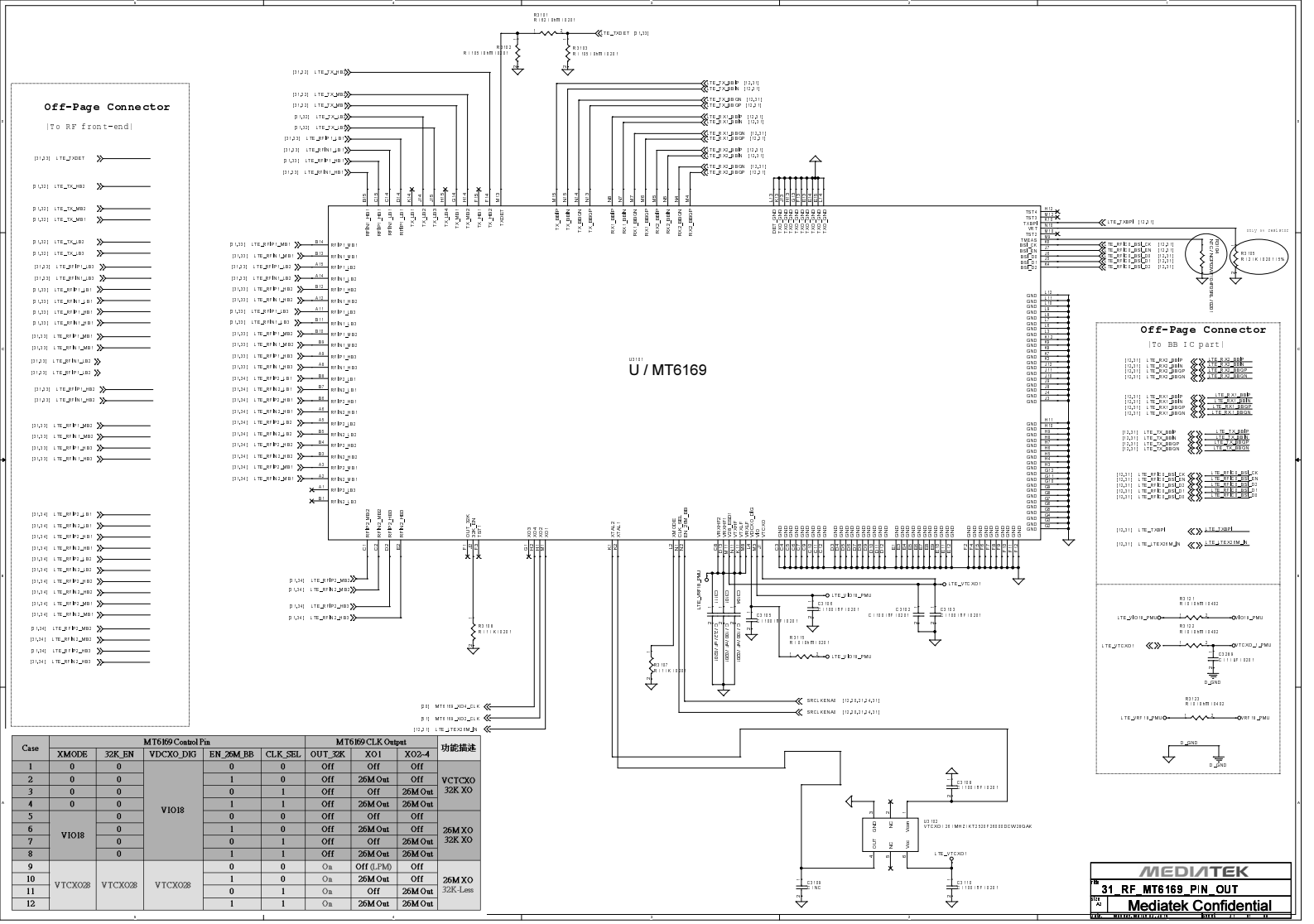
4-Phase Buck

4-Phase Buck I2C address: 0X68 (Write:0xD0, Read:0xD1)



Schematic design notice of "24_POWER_EXT_4PHASE_BUCK" page.

Note 24-1: DA9210's GPIO0 = SRCLKENA0 => Buck EN controlled by SRCLKEN0 or I2C.



Case	MT6169 Control Pin					MT6169 CLK Output			功能描述
	XMODE	32K_EN	VDCXO_DIG	EN_26M_BB	CLK_SEL	OUT_32K	XO1	XO2-4	
1	0	0	VIO18	0	0	Off	Off	Off	VCTCXO 32K XO
2	0	0		1	0	Off	26M Out	Off	
3	0	0		0	1	Off	Off	26M Out	
4	0	0		1	1	Off	26M Out	26M Out	
5	VIO18	0		0	0	Off	Off	Off	26M XO 32K XO
6		0		1	0	Off	26M Out	Off	
7		0		0	1	Off	Off	26M Out	
8		0		1	1	Off	26M Out	26M Out	
9	VTCXO28	VTCXO28	VTCXO28	0	0	On	Off (LPM)	Off	26M XO 32K-Less
10				1	0	On	26M Out	Off	
11				0	1	On	Off	26M Out	
12				1	1	On	26M Out	26M Out	

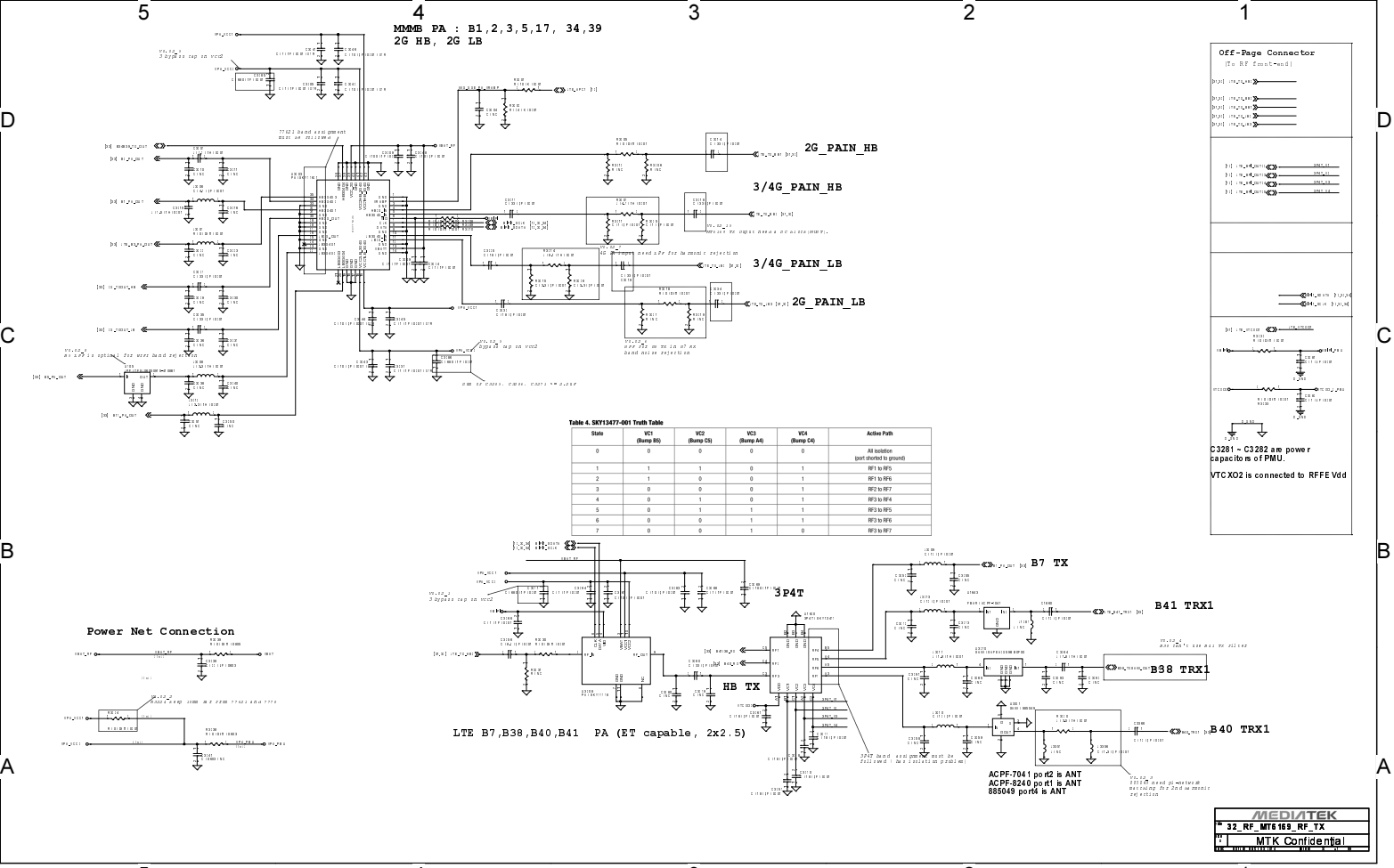
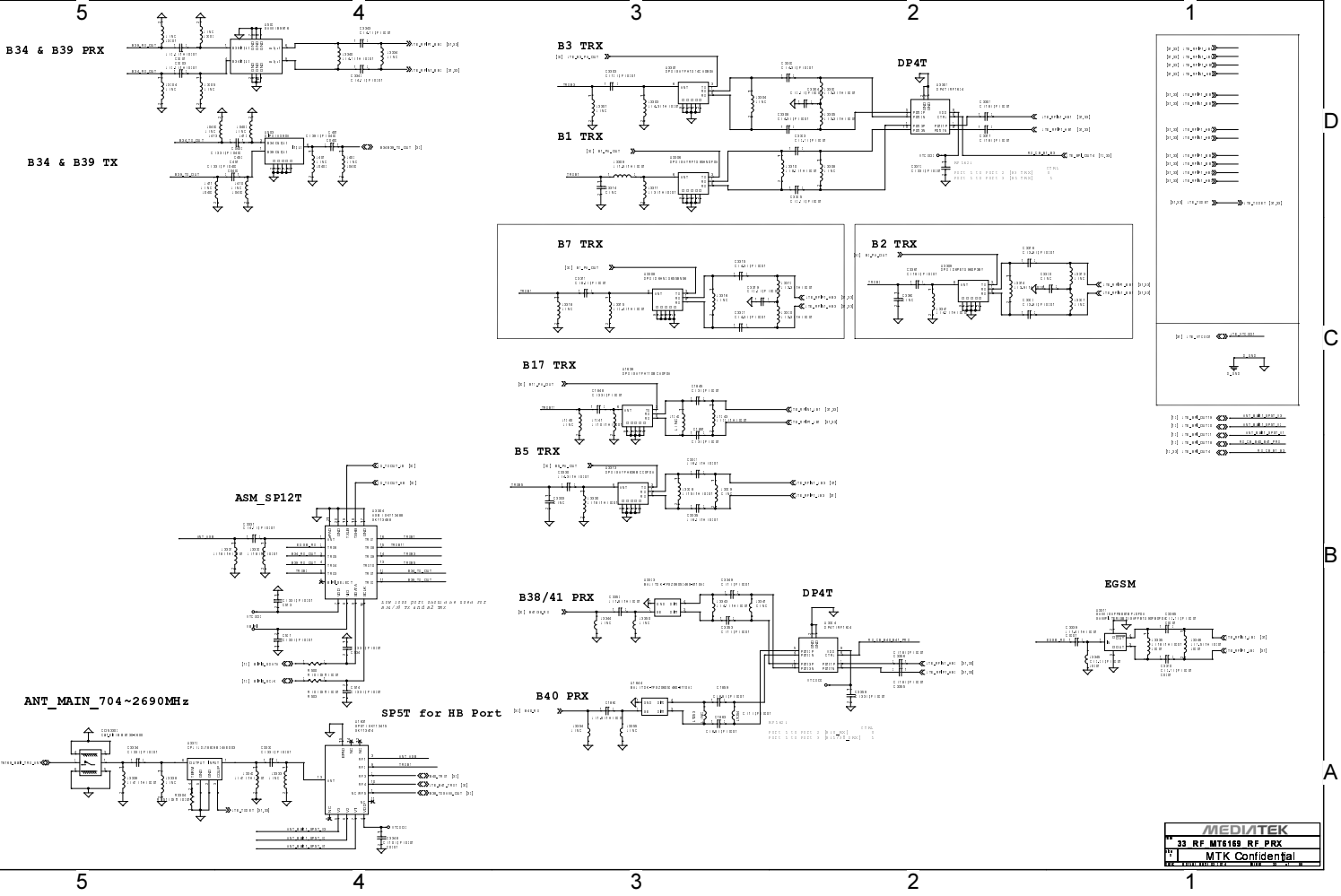


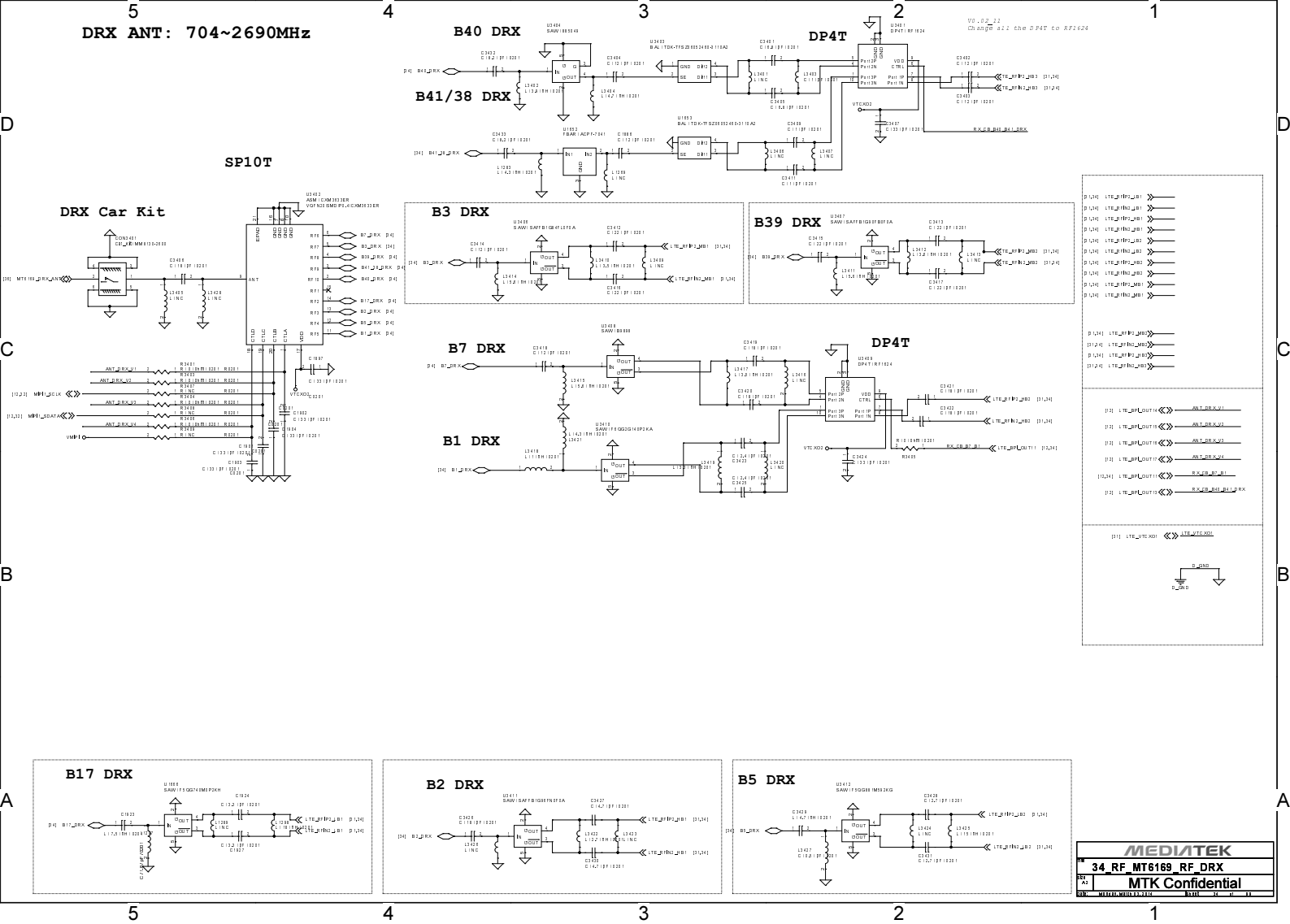
Table 4. SKY13477-001 Truth Table

State	VC1 (Bump B5)	VC2 (Bump C5)	VC3 (Bump A4)	VC4 (Bump C4)	Active Path
0	0	0	0	0	All isolation (port shorted to ground)
1	1	1	0	1	RF1 to RF5
2	1	0	0	1	RF1 to RF6
3	0	0	0	1	RF2 to RF7
4	0	1	0	1	RF3 to RF4
5	0	1	1	1	RF3 to RF5
6	0	0	1	1	RF3 to RF6
7	0	0	1	0	RF3 to RF7

Power Net Connection


B34 & B39 PRX
B34 & B39 TX
B3 TRX
B1 TRX
DP4T
B7 TRX
B2 TRX
B17 TRX
B5 TRX
ASM_SP12T
ANT_MAIN_704~2690MHz
SP5T for HB Port
B38/41 PRX
B40 PRX
DP4T
EGSM

DRX ANT: 704~2690MHz



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34_RF_MT6169_RF_DRX

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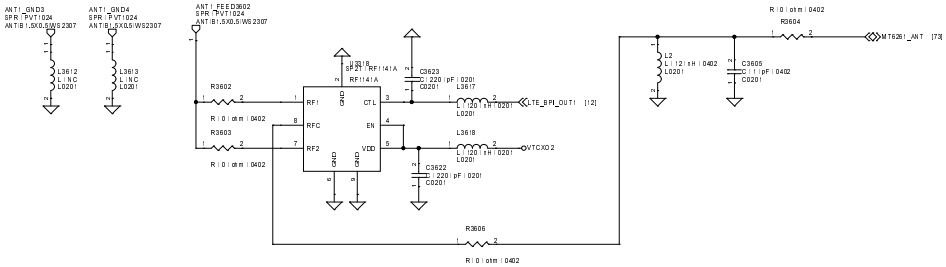
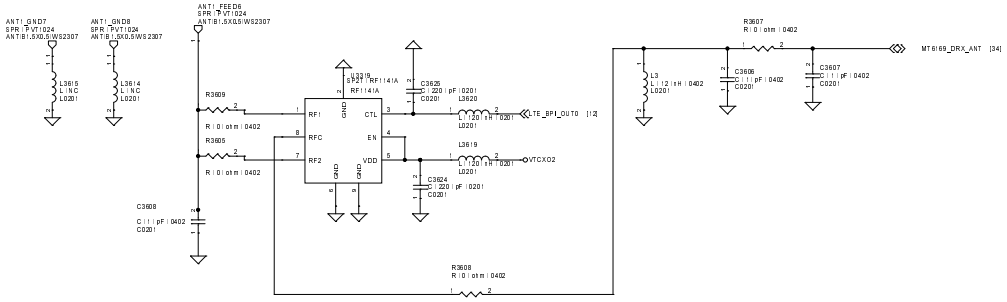
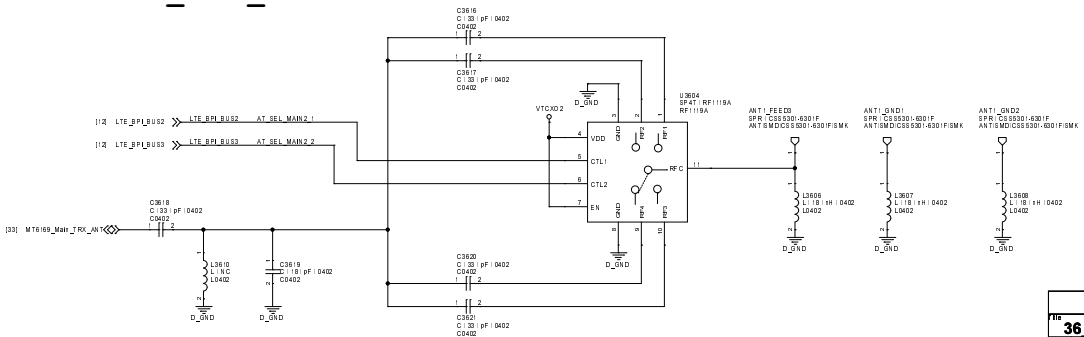
2G Only ANT: 824~960MHz + 1710~1990MHz



DRX ANT: 734~960MHz + 1805~2690MHz



ASM_Main_704~960MHz + 1710~2690MHz



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File: 36_RF_AT

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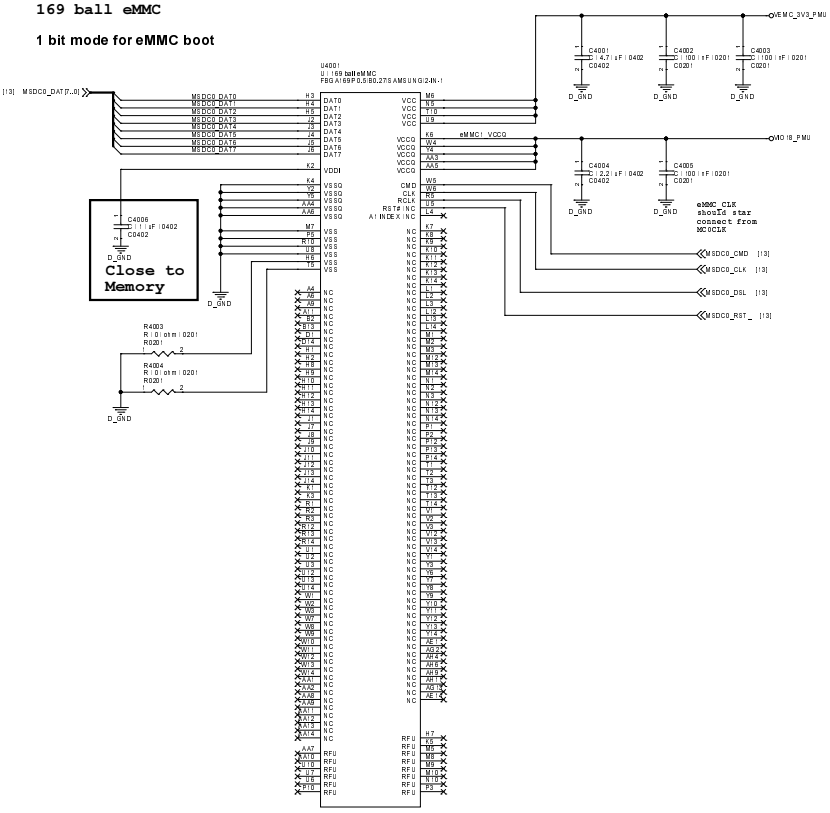
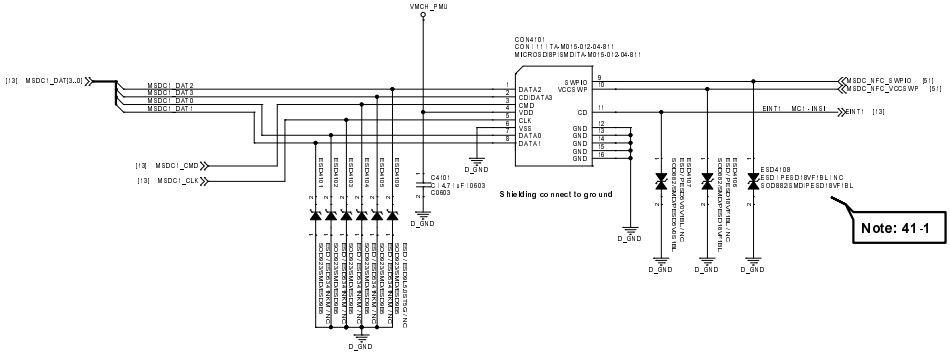
169 ball eMMC

1 bit mode for eMMC boot



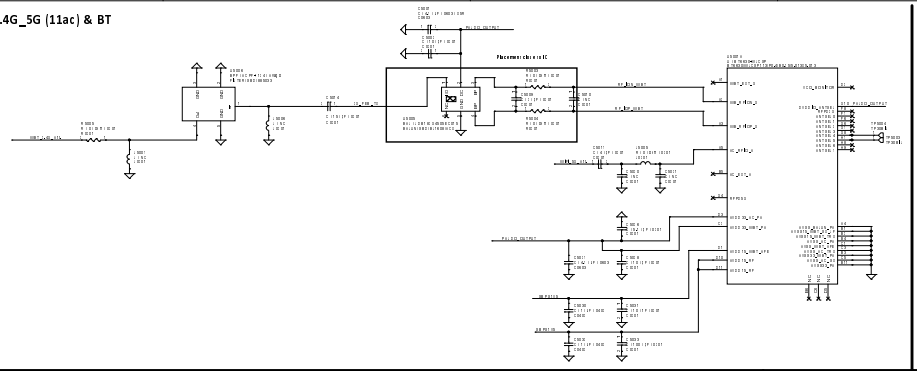
SD CARD



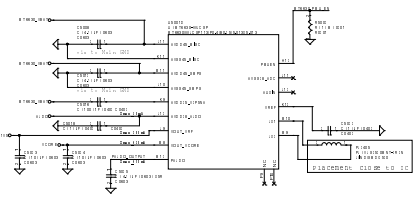
Schematic design notice of "41_MEMORY_SD Card" page.

Note 41-1: The equivalent capacitance of ESD protection device must be <=0.5pF
-- otherwise it will result in NFC card mode function fail.

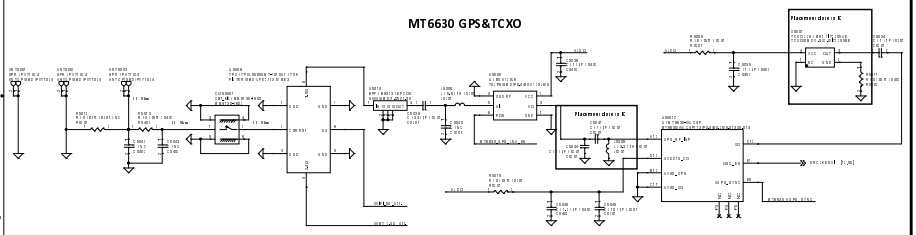
MT6630 WiFi_2.4G_5G (11ac) & BT



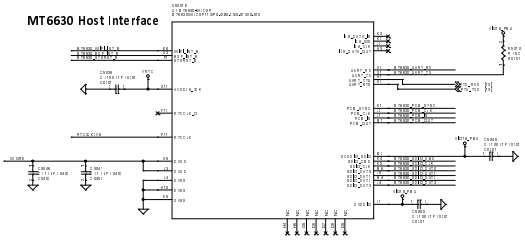
MT6630 PMU



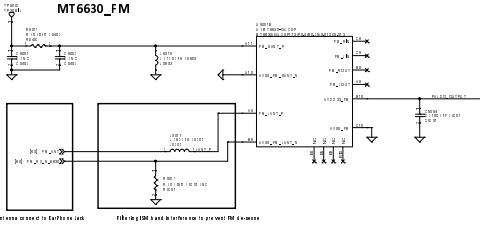
MT6630 GPS&TCXO



MT6630 Host Interface



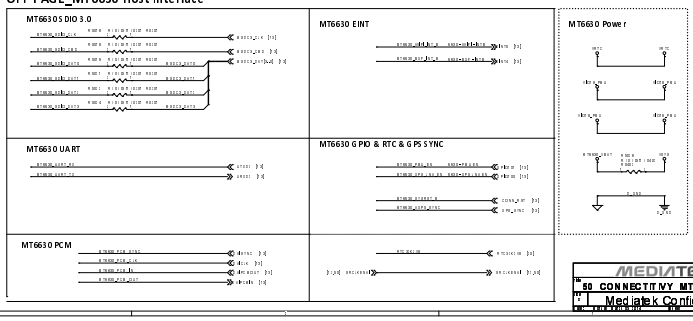
MT6630_FM



FM Long Antenna connect to Earphone jack

Filter long FM band interference to prevent FM de-sense

OFF-PAGE_MT6630 Host Interface

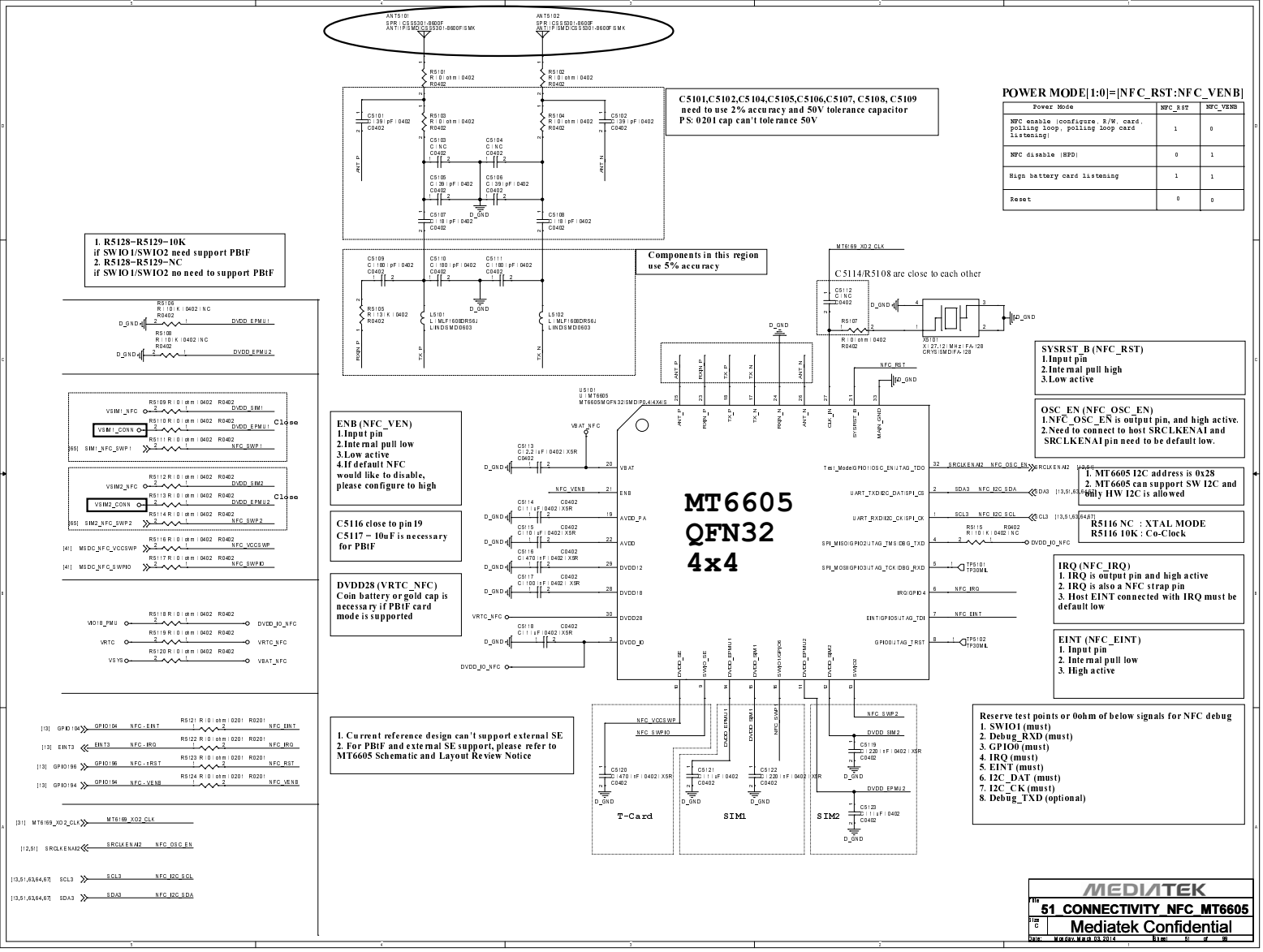


MEDIATEK

Title: 50_CONNECTIVITY_MT6630

Size: C | Mediatek Confidential

Date: | Sheet: | of:


C5101,C5102,C5104,C5105,C5106,C5107, C5108, C5109 need to use 2% accuracy and 50V tolerance capacitor
PS: 0201 cap can't tolerance 50V
POWER MODE[1:0]=[NFC_RST:NFC_VENB]
Power Mode | NFC_RST | NFC_VENB
NFC enable (configure, R/W, card, polling loop, polling loop card listening) | 1 | 0
NFC disable (RPD) | 0 | 1
High battery card listening | 1 | 1
Reset | 0 | 0
1. R5128~R5129~10K if SWIO1/SWIO2 need support PBtF
2. R5128~R5129~NC if SWIO1/SWIO2 no need to support PBtF
Components in this region use 5% accuracy
C5114/R5108 are close to each other
SYSRST_B (NFC_RST)
1.Input pin
2.Internal pull high
3.Low active
OSC_EN (NFC_OSC_EN)
1.NFC_OSC_EN is output pin, and high active.
2.Need to connect to host SRCLKENAI and SRCLKENAI pin need to be default low.
ENB (NFC_VEN)
1.Input pin
2.Internal pull low
3.Low active
4.If default NFC would like to disable, please configure to high
1. MT6605 I2C address is 0x28
2. MT6605 can support SW I2C and only HW I2C is allowed
C5116 close to pin19
C5117 ~ 10uF is necessary for PBtF
R5116 NC : XTAL MODE
R5116 10K : Co-Clock
DVDD28 (VRTC_NFC)
Coin battery or gold cap is necessary if PBtF card mode is supported
IRQ (NFC_IRQ)
1. IRQ is output pin and high active
2. IRQ is also a NFC strap pin
3. Host EINT connected with IRQ must be default low
EINT (NFC_EINT)
1. Input pin
2. Internal pull low
3. High active
MT6605
QFN32
4x4
1. Current reference design can't support external SE
2. For PBtF and external SE support, please refer to MT6605 Schematic and Layout Review Notice
Reserve test points or 0ohm of below signals for NFC debug
1. SWIO1 (must)
2. Debug_RXD (must)
3. GPIO0 (must)
4. IRQ (must)
5. EINT (must)
6. I2C_DAT (must)
7. I2C_CK (must)
8. Debug_TXD (optional)
T-Card
SIM1
SIM2
MEDIATEK
File
51_CONNECTIVITY_NFC_MT6605
Size C
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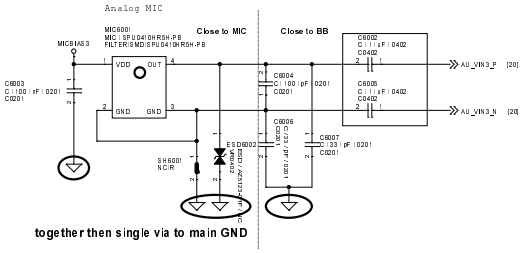
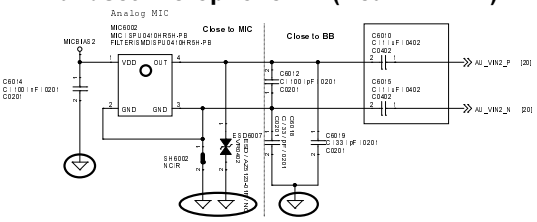
Handset Microphone 1 (Front - ANC)



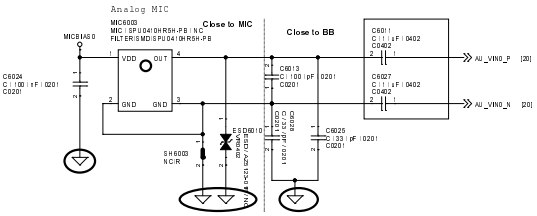
together then single via to main GND

Handset Microphone 2-1 (Rear - DMNR)



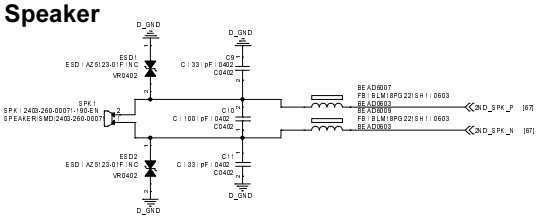
together then single via to main GND

Main microphone

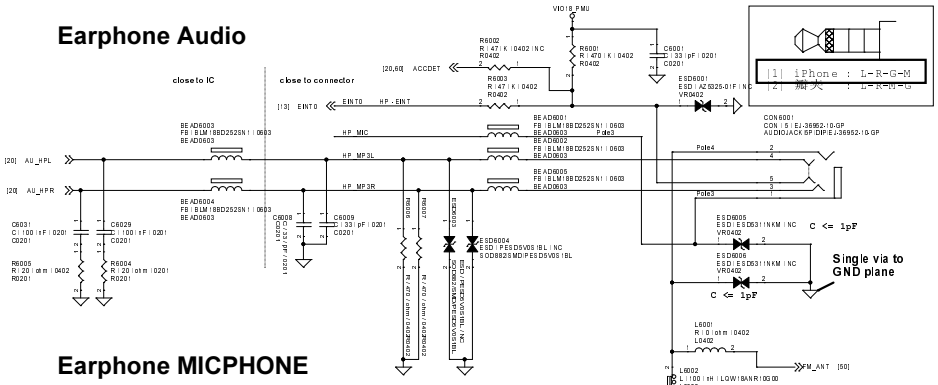


together then single via to main GND

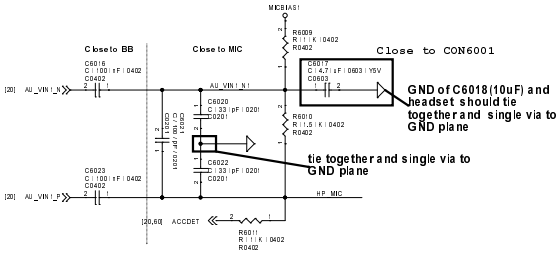
Speaker



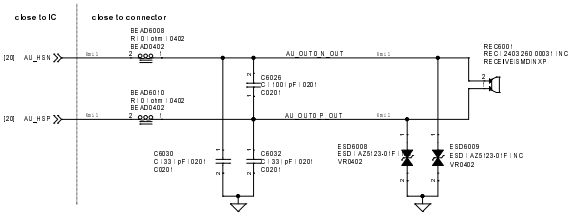
Earphone Audio



Earphone MICPHONE



Receiver



MEDIATEK

File: 60_PERI_AUDIO_IO

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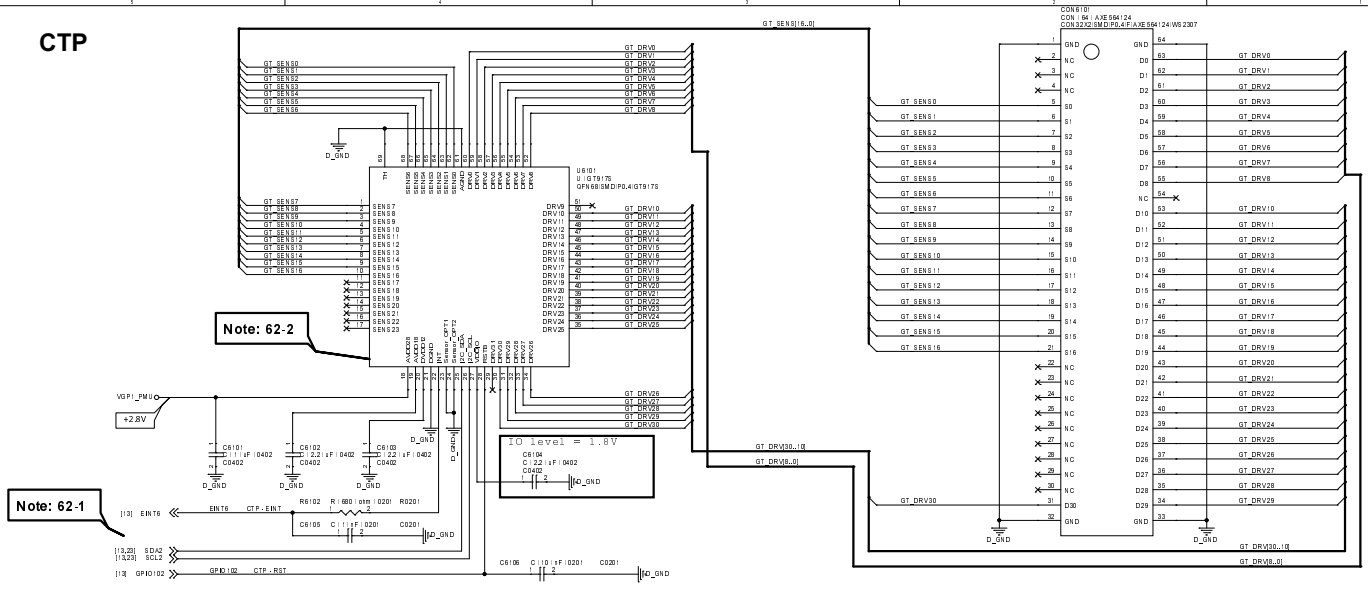
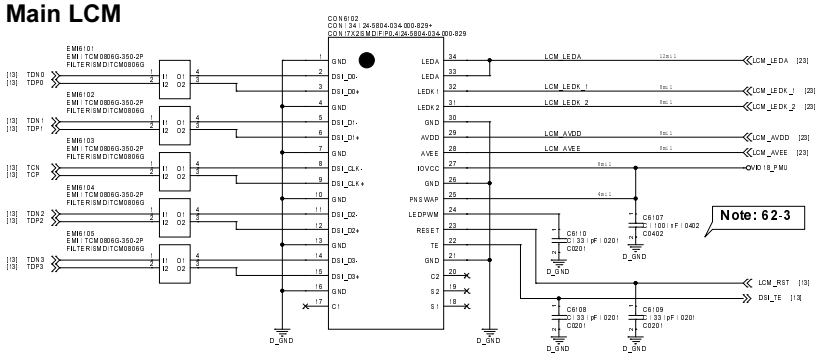
CTP



Main LCM



Schematic design notice of "62_PERI_LCD_CTP" page.

Note 62-1:	GT917S I2C address: 0X5D (Write:0xBA, Read:0xBB)
Note 62-2:	Connect GT917S's "Sensor_OPT1 & 2" pins to GND for COB application. GT917S's INT pin CANNOT be pulled-up.
Note 62-3:	PNSWAP are used for the polarity swap of MIPI. PNSWAP=IOVCC => DP=DP,DN=DN;

MEDIATEK

File: 61_PERI_LCD_CTP

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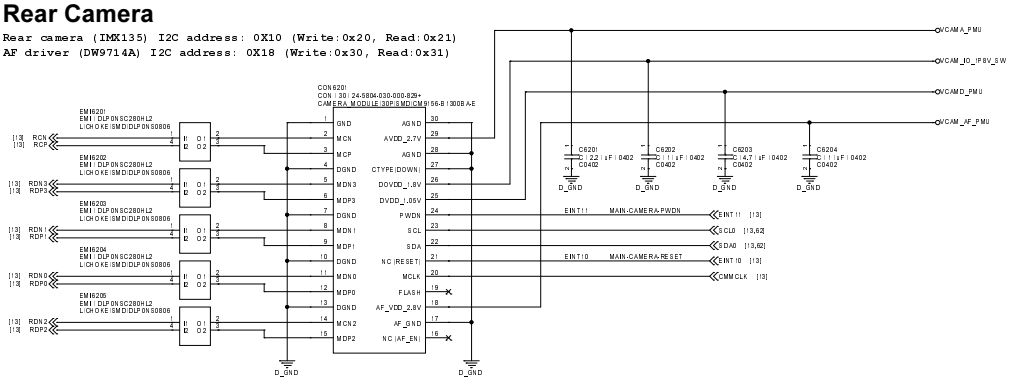
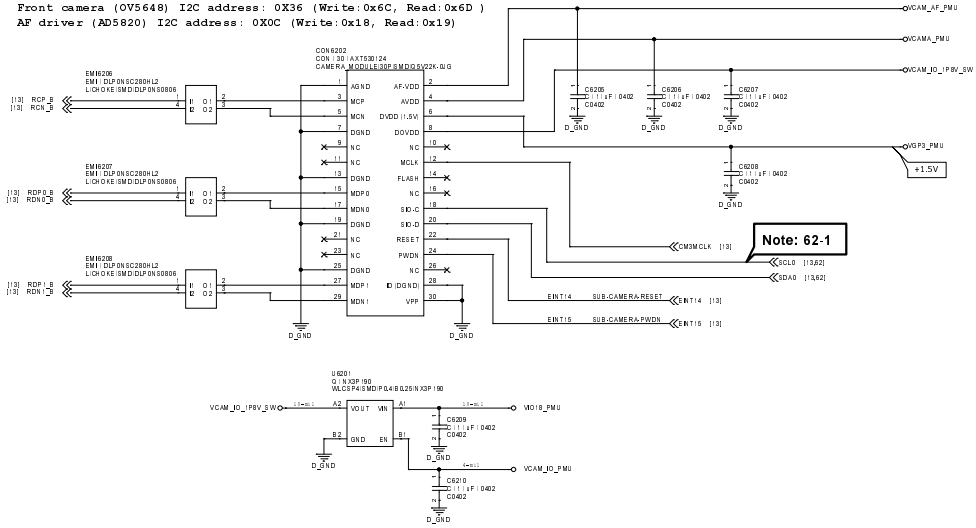
Rear Camera

Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21)
AF driver (DW9714A) I2C address: 0X18 (Write:0x30, Read:0x31)



Front Camera

Front camera (OV5648) I2C address: 0X36 (Write:0x6C, Read:0x6D)
AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)

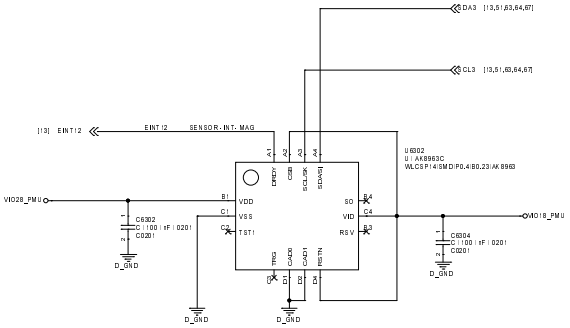


Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

Note 62-1: The VCC of I2C_0 is pulled to "VCAM_IO_PMU".

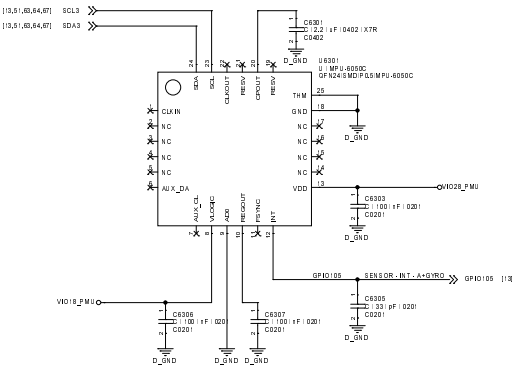
M-Sensor

M-Sensor I2C Address: 0x0C (Write:0x18, Read:0x19)



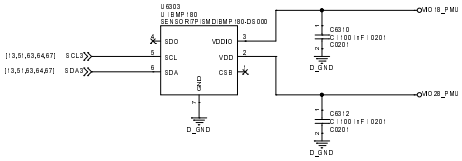
Accerometer + Gyro Sensor

A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)



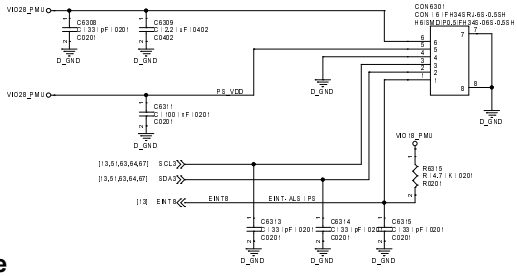
Pressure Sensor

Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)

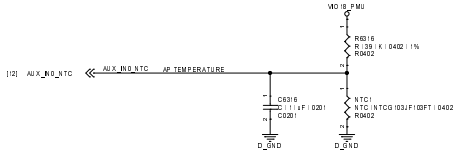


RGB & PS Sensor

CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1)



Thermister / To sense board level temperature



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File	63_PERI_SENSORS
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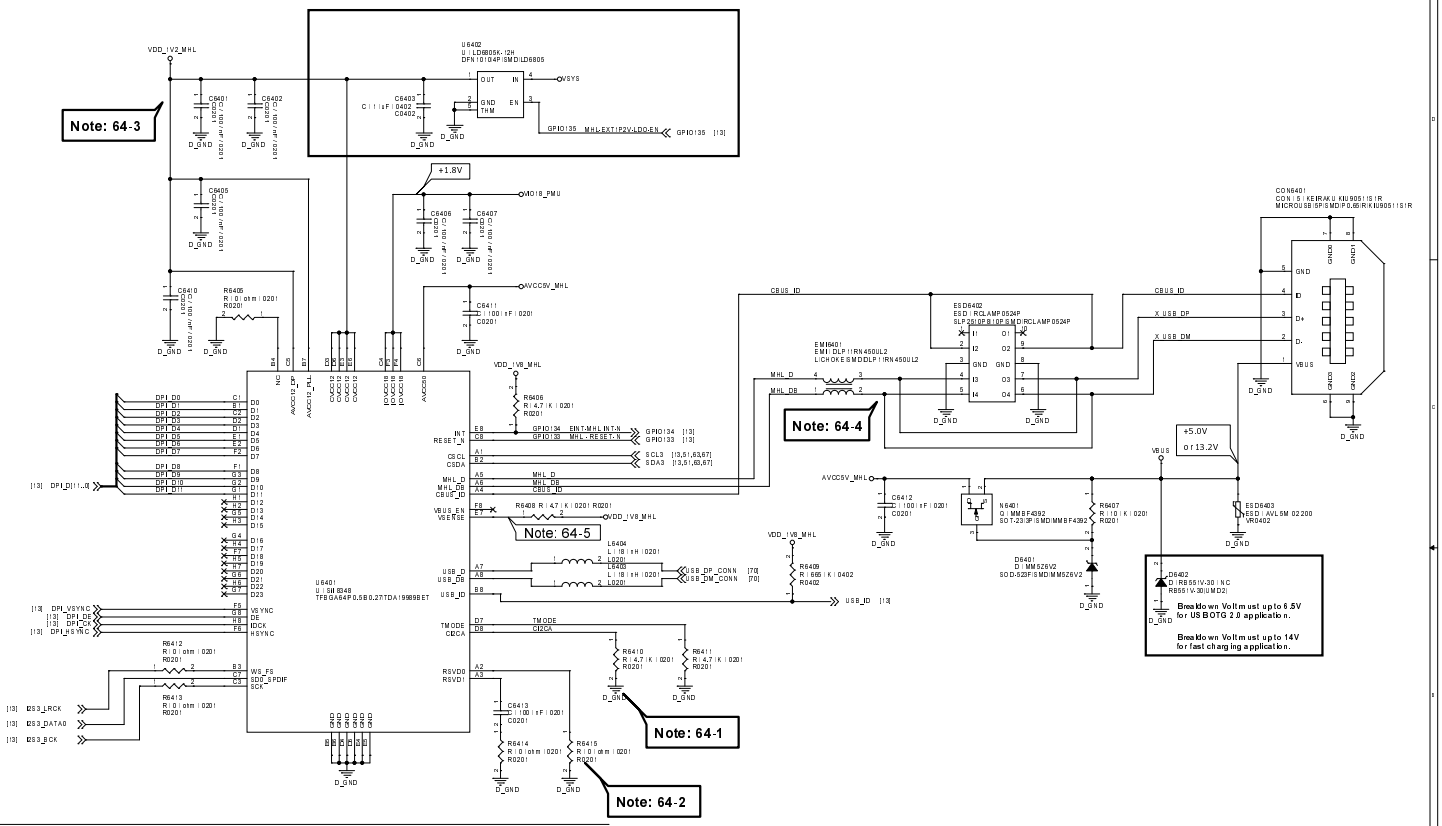

Schematic design notice of "64_PERI_USB_MHL" page.

Note 64-1: CI2CA High : MHL I2C Address = 0x3B/3F/4F. (Write:0x76/7E/9E, Read:0x77/7F/9F)
CI2CA Low : MHL I2C Address = 0x39/3D/4D. (Write:0x72/7A/9A, Read:0x73/7B/9B)

Note 64-2: 1. To reserve one 0ohm resistor to GND for ball A2.
2. To reserve one 0.1uF cap + one 0ohm resistor to GND in serial connection for ball A3.

Note 64-3: 1. Please reserve power bead among CVCC12, AVCC12_PLL and AVCC12_DP.
2. Please add 10Kohm resistor to GND for NC ball B4.

Note 64-4: Please add one CMC on MHL diff pair which could help filter the noise and increase the clock/data rise/fall time.

Note 64-5: Please connect 1V8 for ball E7

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File: 64_PERI_USB_MHL
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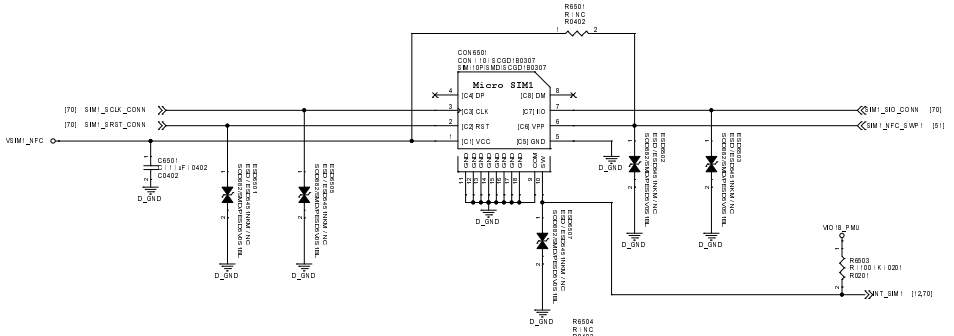
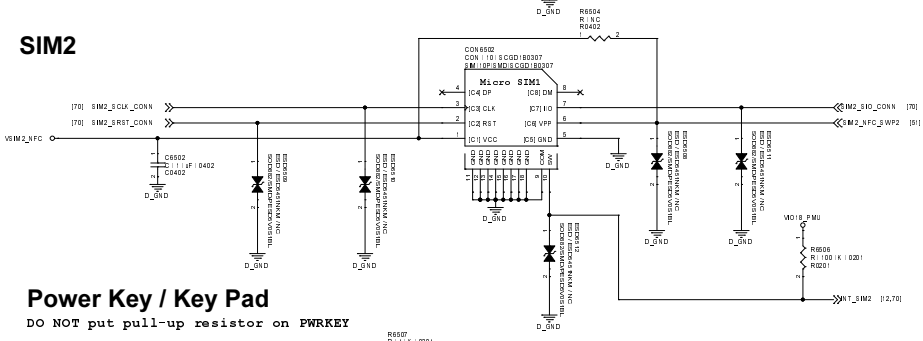
SIM1 & SmartCard

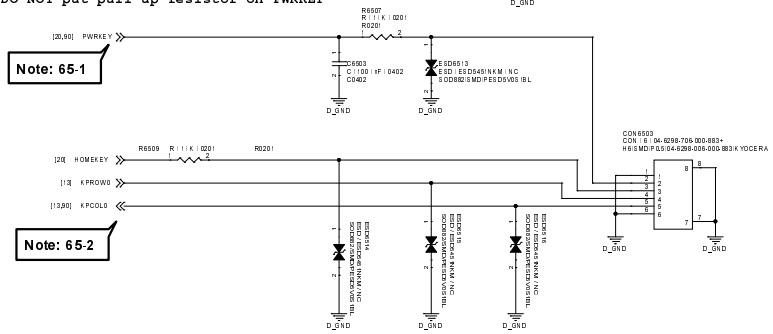


SIM2



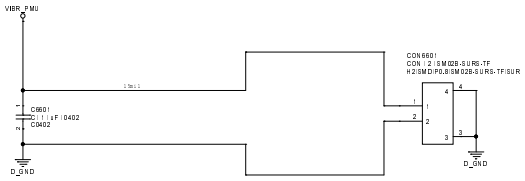
Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.
Note 65-1: DO NOT put pull-up resistor on PWRKEY
Note 65-2: Volume Up : (KPROW0/KPCOL0) Or HOME Key / GND Volume Down : (KPROW0/KPCOL1) Or KPCOL0 / GND

VIBRATOR



MEDIATEK

File: 66_PERI_VIBRATOR

Size: C

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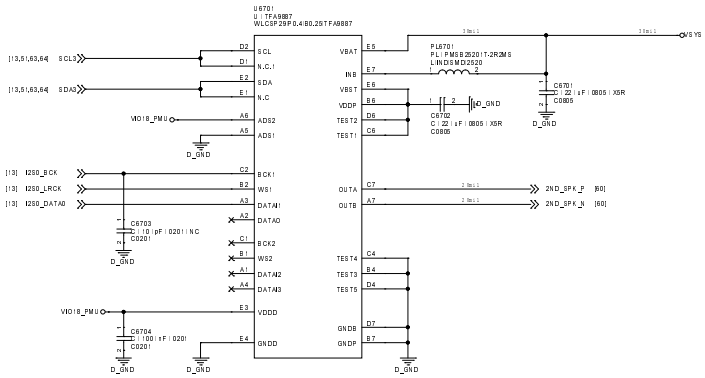
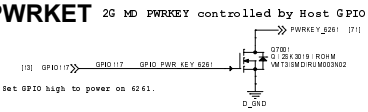
Speaker Amplifier

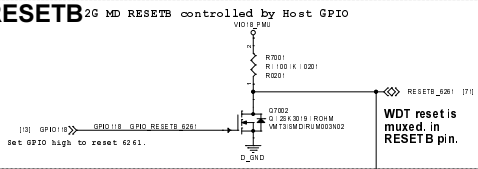
Speaker AMP I2C Address: 0x36 (Write:0x6C, Read:0x6D) when ADS1 = GND; ADS2 = VDD.



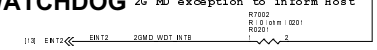
PWRKET
2G MD PWRKEY controlled by Host GPIO



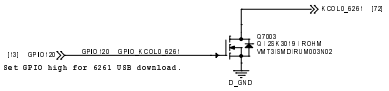
RESETB
2G MD RESETB controlled by Host GPIO



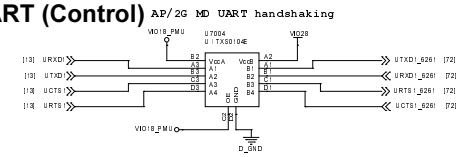
WATCHDOG
2G MD exception to inform Host



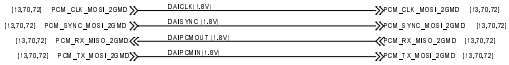
KCOL0
2G MD USB download when tie to GND



UART (Control)
AP/2G MD UART handshaking



PCM (Speech)



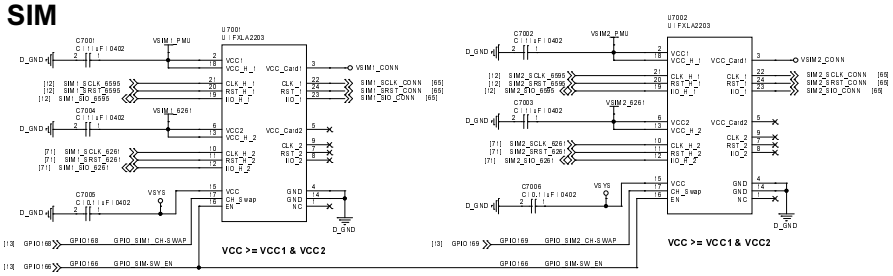
WAKEUP
Host wake up 2G MD

WAKEUP
2G MD wake up Host

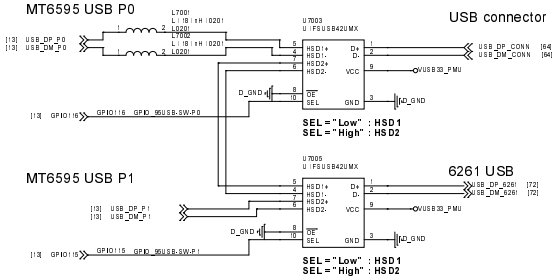
MD EXP
2G MD exception to inform Host

RF

SIM

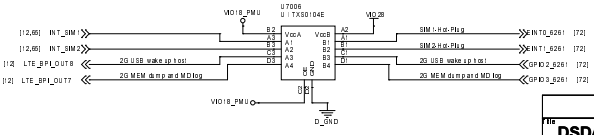


USB



MT6595's GPIO116 (GPIO_95USB-SW-P0	MT6595's GPIO115 (GPIO_95USB-SW-P1	Function description	HW default setting
0	0	USB CONN <=> MT6595 USB P0. MT6261 USB <=> NC.	
0	1	USB CONN <=> MT6595 USB P0. MT6261 USB <=> MT6595 USB P1	V
1	0	USB CONN <=> MT6261 USB for 6261 firmware upgrade via PC.	
1	1	USB CONN <=> NC MT6261 USB <=> MT6595 USB P1	

INTs



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File: DSDA Interface

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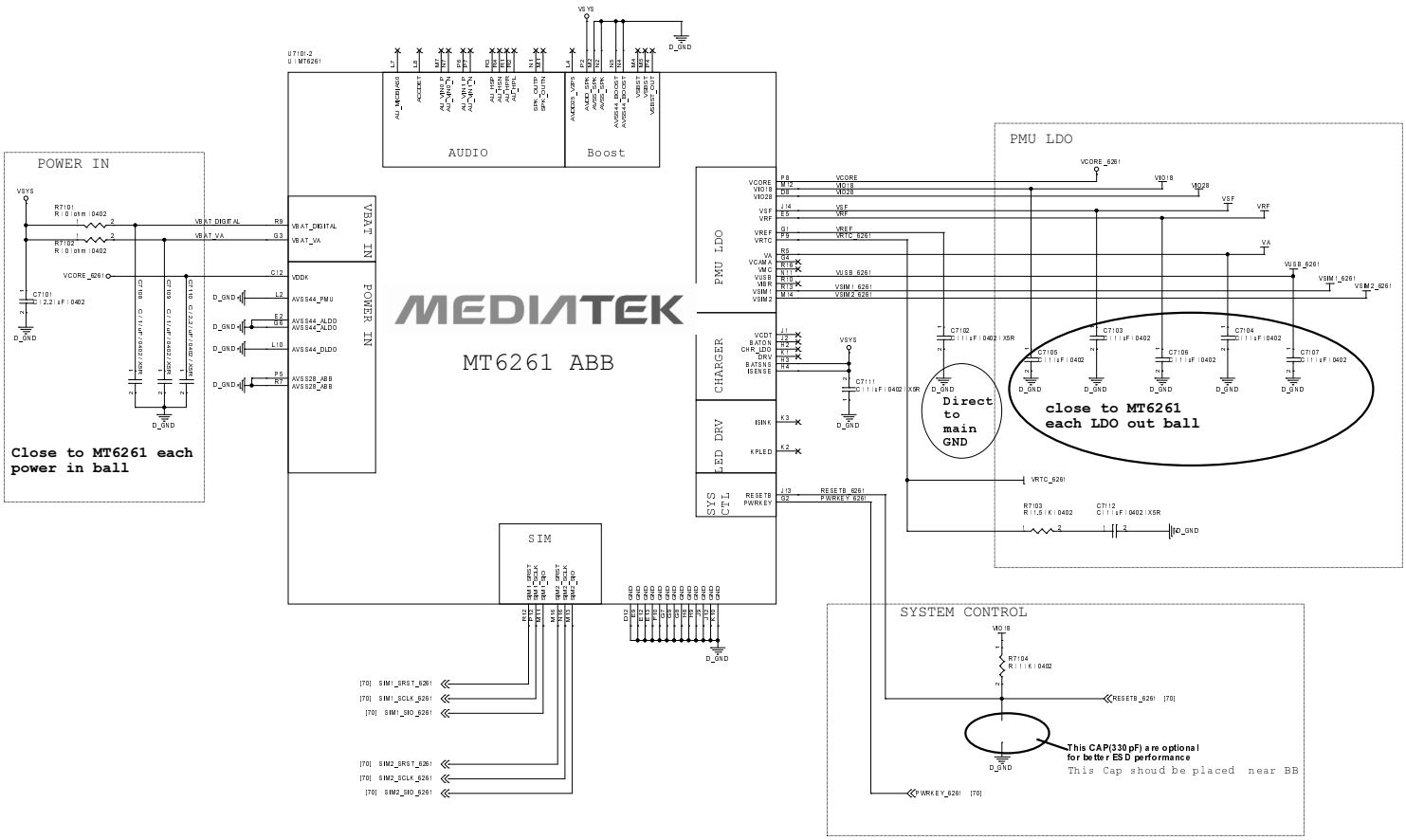

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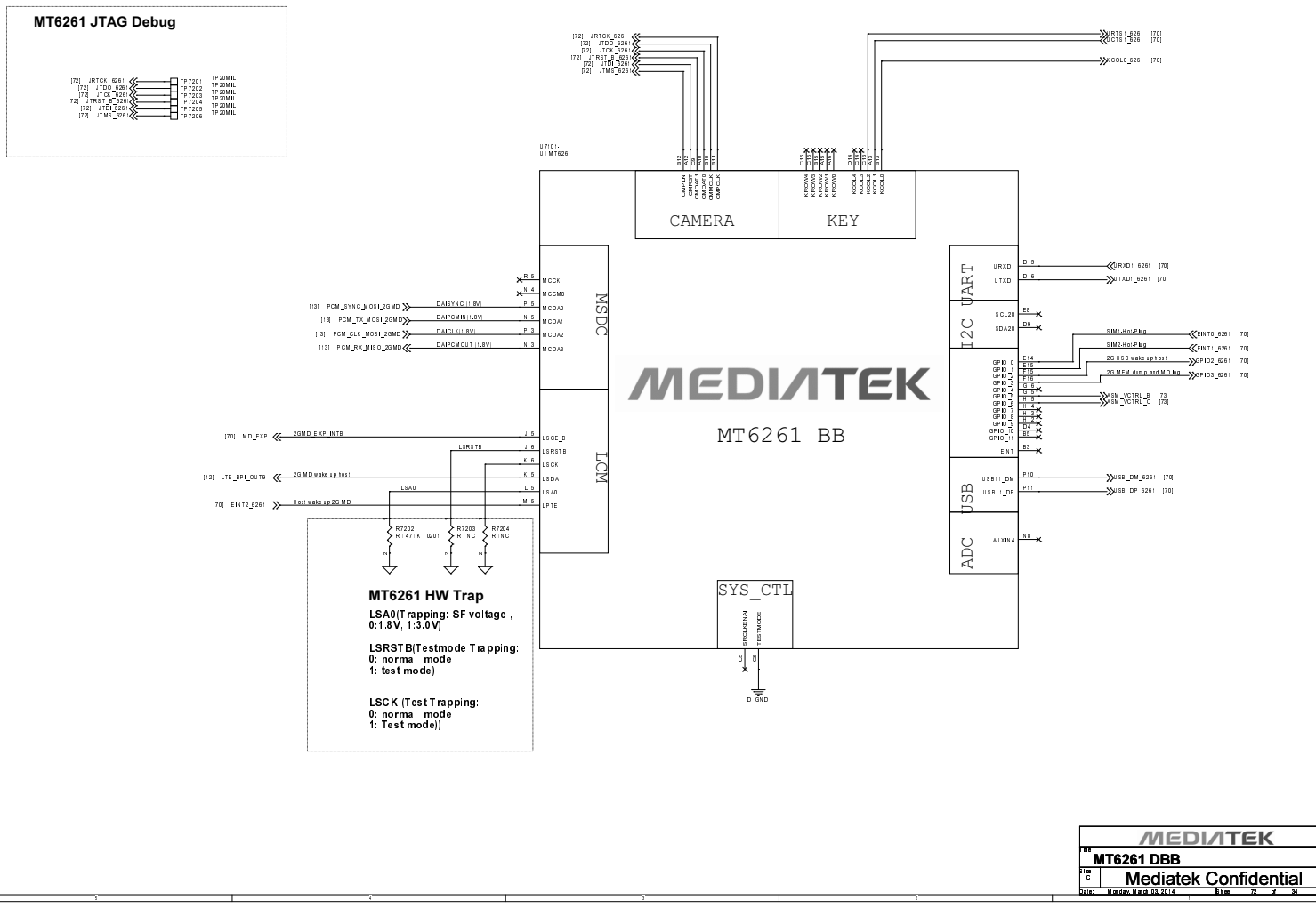

MEDIATEK

File: MT6261 DBB

Size: C — Mediatek Confidential

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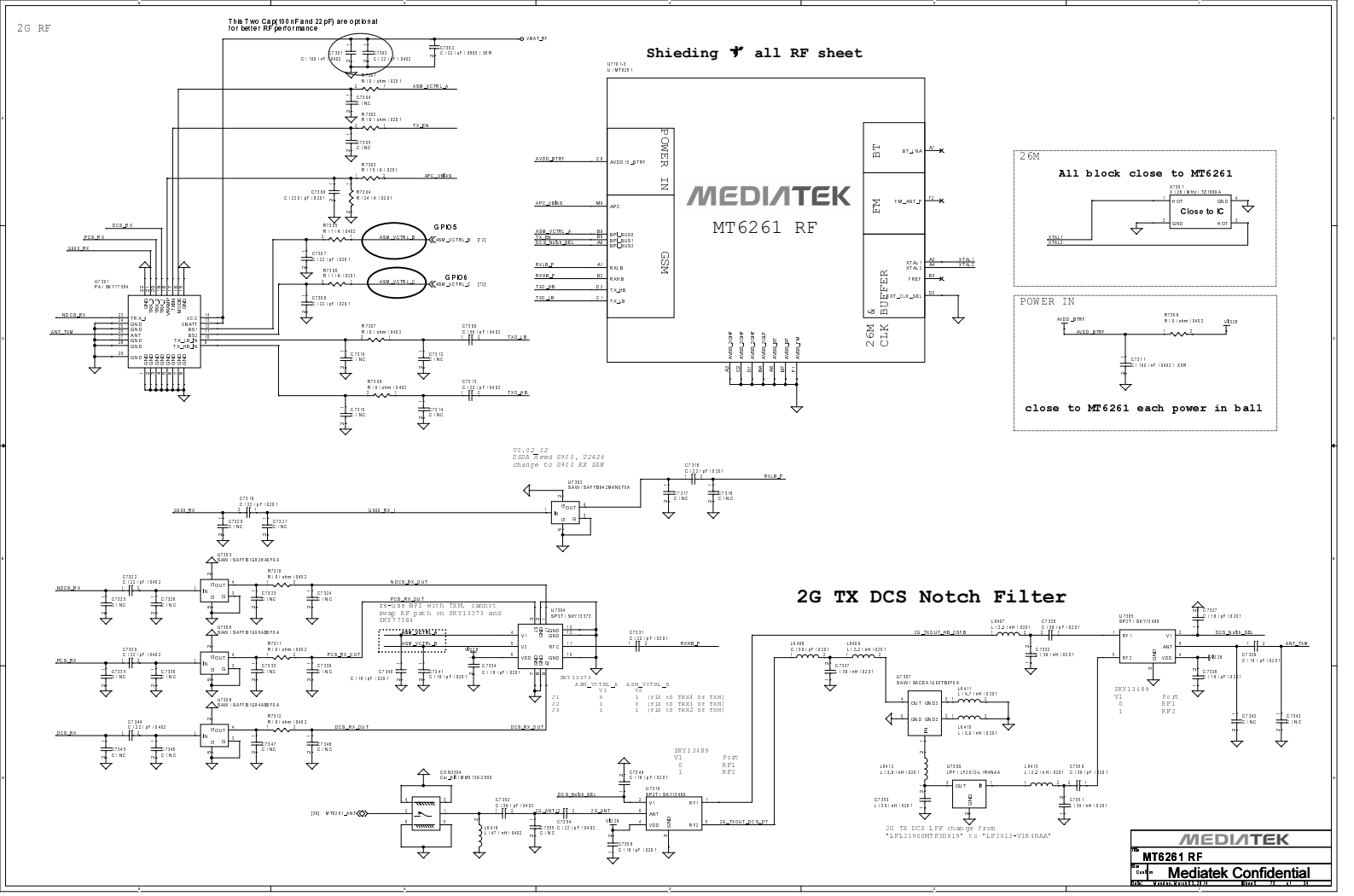
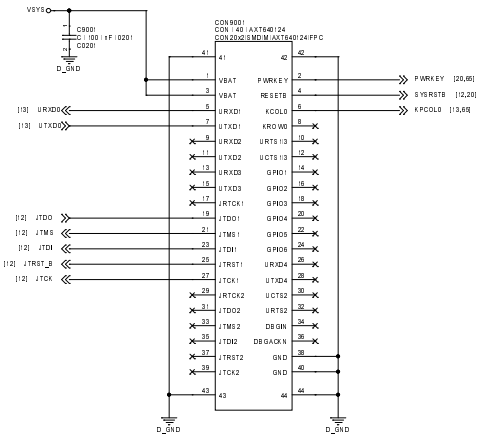


2G TX DCS Notch Filter



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