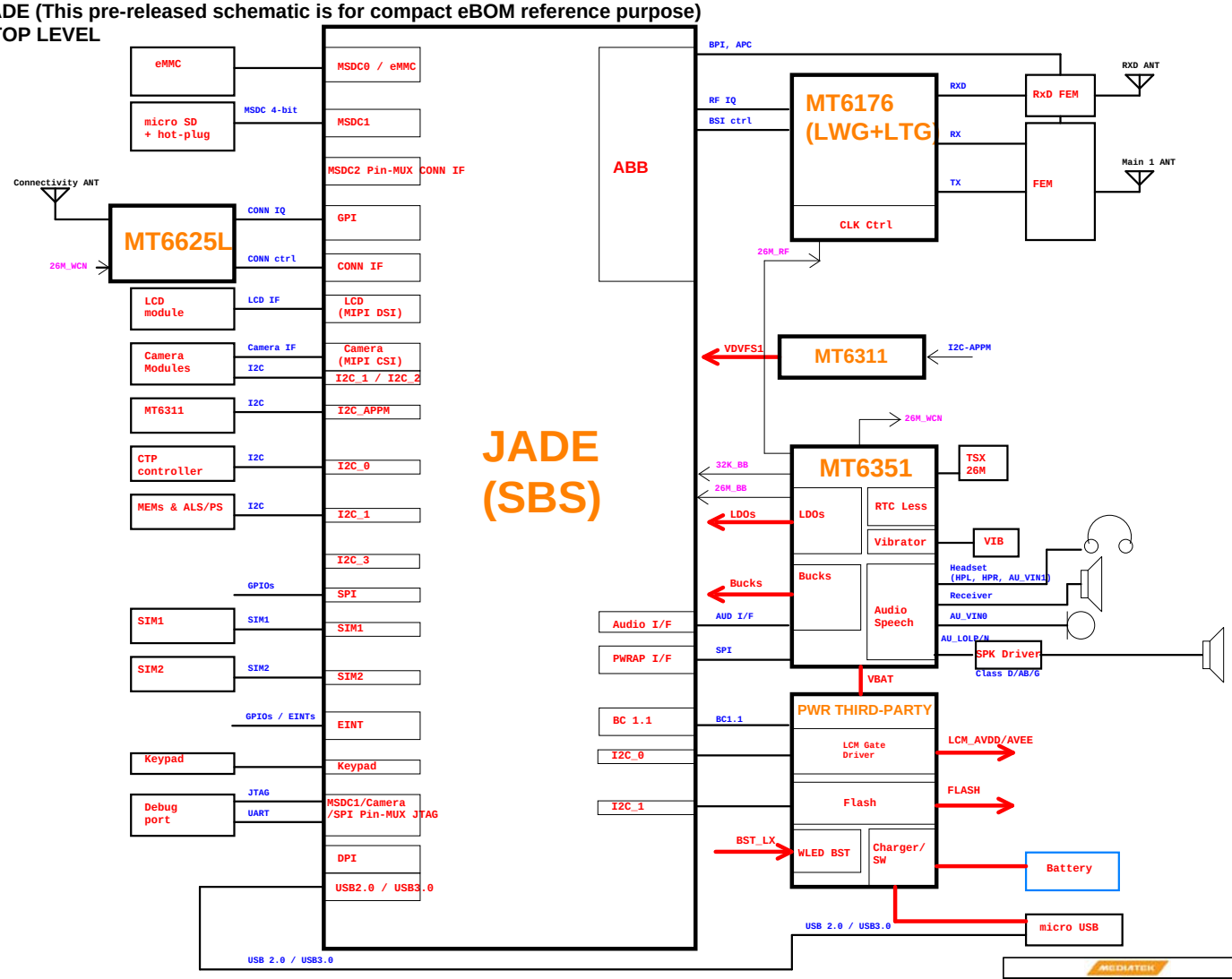
Project : JADE (This pre-released schematic is for compact eBOM reference purpose)
REF_SCH TOP LEVEL



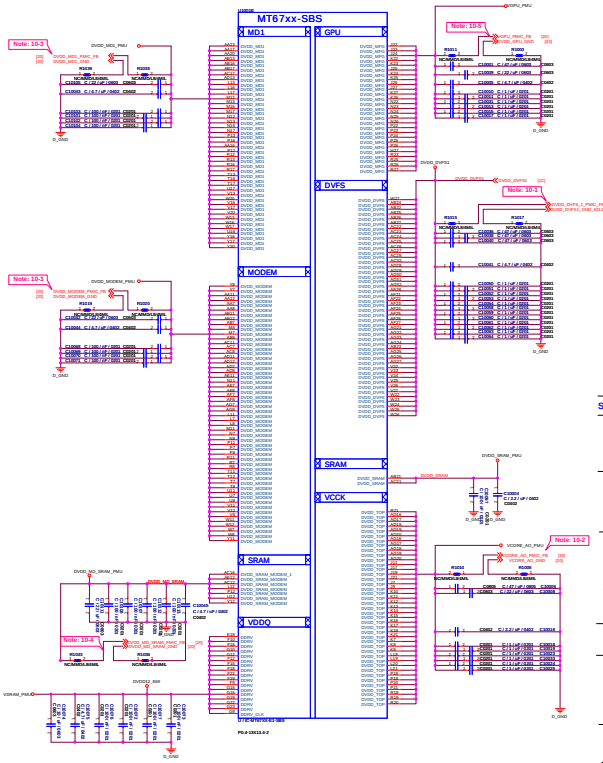
This pre-released schematic is for compact eBOM reference purpose

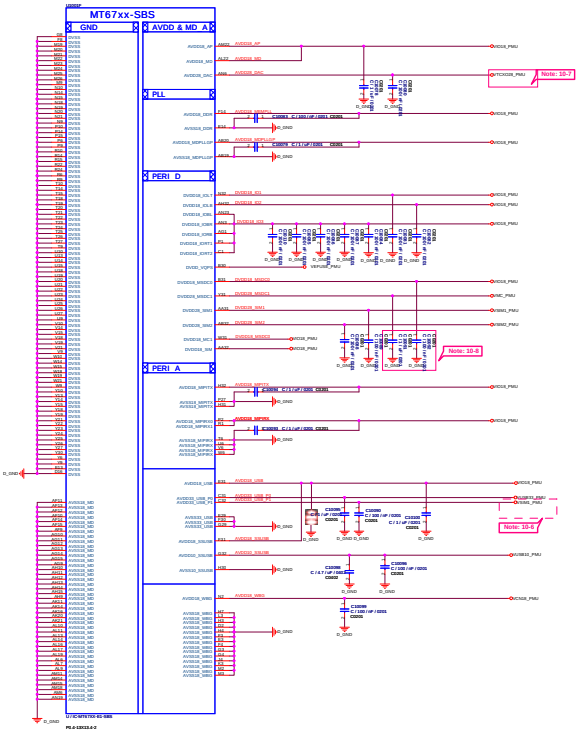
MEDIATEK

File	01_Block_Diagram
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 01 of 99

I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	CTP	400 Kbps	Yes.	GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
	LCM Gate Driver	400 Kbps		NT50358 / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
I2C-1	M Sensor	400 Kbps		YAS533 / M-Sensor I2C Address 0x2E (Write: 0x5C, Read: 0x5D)
	A+Gyro Sensor	400 Kbps	Yes.	MPU-6515 / A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Baro Sensor	400 Kbps		BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	RGB / PS Sensor	400 Kbps		CM36558/ RGB+PS I2C address: 0x51 (Write:0x TBC, Read:0xTBC)
	Flash LED	400 Kbps		RT4505 / Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)
	Front Camera	400 Kbps	Yes.	Front camera (OV5648) I2C address: 0X36 (Write:0x6C, Read:0x6D) AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)
	SWCHR	400 Kbps	TBD	BQ25896/ SWCHR I2C address: 0X6B (Write:0xTBC, Read:0xTBC)
I2C-2	Rear Camera - 13M	400 Kbps	Yes.	Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (DW9714A) I2C address: 0X18 (Write:0x30, Read:0x31)
	Rear Camera - 16M	400 Kbps	Yes.	TBD AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-3	NC			
I2C-APPM	MT6311	TBD	Yes.	MT6311 / 2-Phase Buck I2C address: 0X6B (Write:0x, Read:0x)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode Plus (1 Mbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)





Schematic design notice of "10_BB_POWER" page.

Note 10-1: 4 mil GND trace with good shielding to PMIC (Differential)

Differential pair of DVFS1 remote sense must be close to BB´s ball.

Note 10-2: VCORE_AO remote sense must be close to BB´s ball.

Remote sense trace with GNDshielding to PMIC (Differential)

Note 10-3: DVDD_MD1 and DVDD_MODEM remote sense must be close to BB´s ball.

Remote sense trace with GNDshielding to PMIC (Differential)

Note 10-4: VDRAM remote sense must be close to BB´s ball.

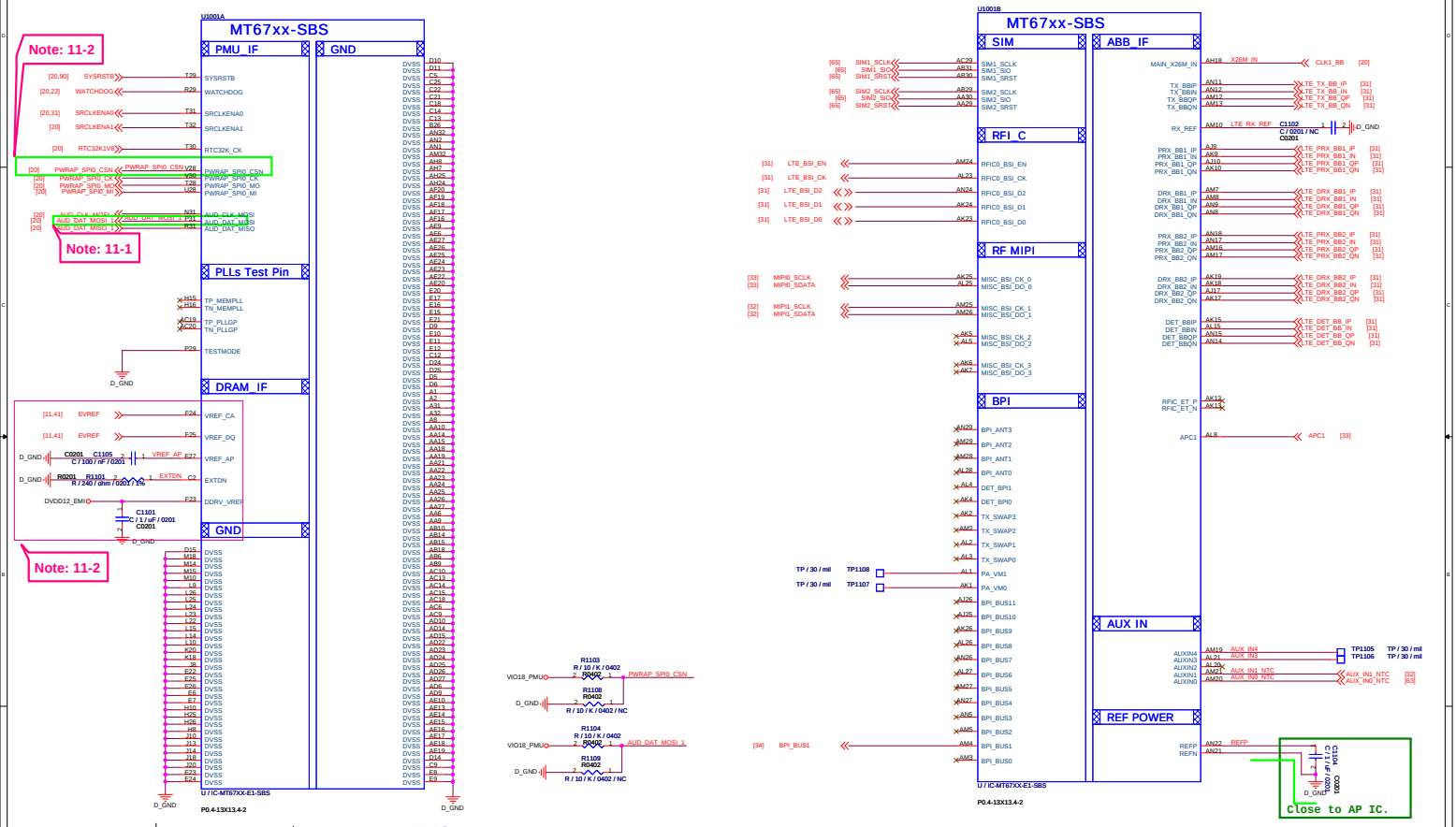
Note 10-5: Differential pair of GPU remote sense must be close to BB´s ball.

Note 10-6: Connect AVDD33_USB_P1 (C32 ball) to "VSIM1_PMU" for IC-USB / Samrt card application.

Connect AVDD33_USB_P1 (C32 ball) to "VUSB33_PMU" for USB application.

Note 10-7: AVDD28_DAC (AN6 ball) must be powered by "VTCXO28_PMU".

Note 10-8: C10091 closed DVDD28_MSDC1 150mil
C10092 closed DVDD18_MSDC0 150mil



PWRAP_SPI0_CSN	AUD_DAT_MOSI	JTAG
HI	LO	N/A
HI	HI	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI
LO	LO	CAM_PDN0/CAM_PDN1/CAM_RST0/CAM_RST1
LO	HI	MSDC1_CLK/MSDC1_CMD/MSDC1_DAT0/MSDC1_DAT1

Schematic design notice of "11_BB_1" page.

Note 11-1: PWRAP_SPI0_CSN and AUD_DAT_MOSI are JTAG feature in bootstrap.

Note 11-2: The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible.

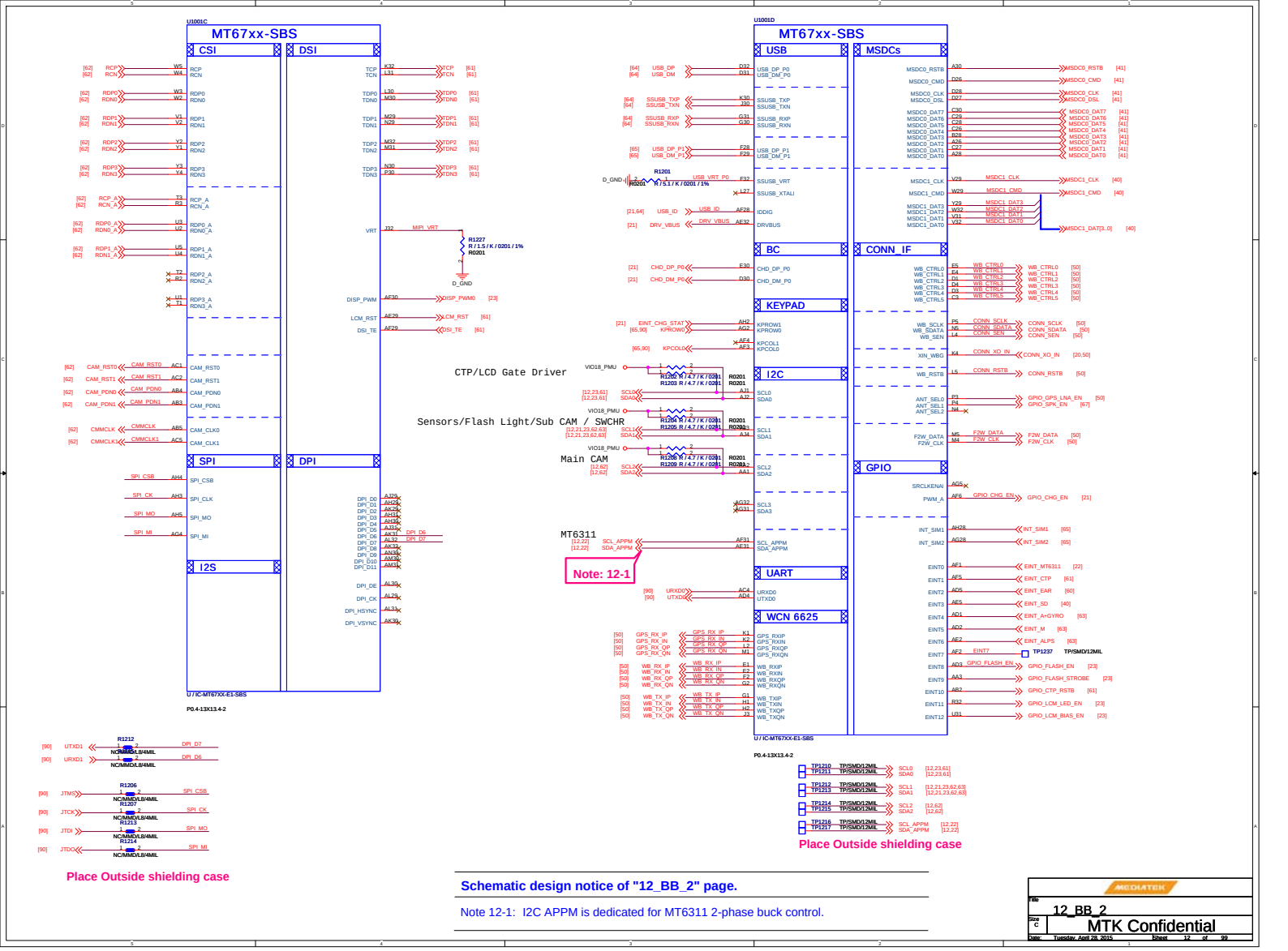
MEDIATEK

File: 11_BB_1

Size: C

MTK Confidential

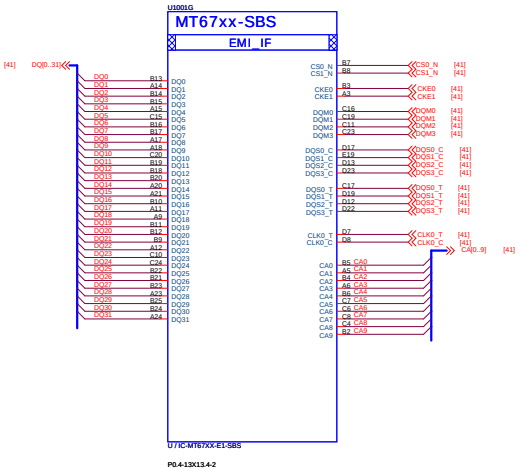
Date: Tuesday, April 28, 2015 Sheet 11 of 99



Schematic design notice of "12_BB_2" page.

Note 12-1: I2C APPM is dedicated for MT6311 2-phase buck control.

Title	12_BB_2
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 12 of 99



MEDIATEK

File	13_BB_3
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 13 of 99

BUCK

Schematic design notice of "20_POWER_MT6351" page.

Note 20-1: Layout trace from MT6351 ball G4 AUDREFN to Audio jack GND must surround shield with GND

Note 20-2: Route AUXADC_REF/AUXADC_TSX as differential trace (4 mil each)with well GND shielding and route AUXADC_GND with 20mil trace width under AUXADC_TSX/AUXADC_REF trace to provide return current path.

VMODEM:0.5V~1.4V/1.2A

VGPU:0.5V~1.4V/3A

VCORE:0.5V~1.4V/3A

VMD1:1V/1.2A

VSRAM_MD:0.8V~0.9V/1.2A

VS1:2V/2A

VS2:1.4V/2A

VPA:0.5V~3.4V/800mA

Note: 20-2

Note: 20-1

Close to MT6351

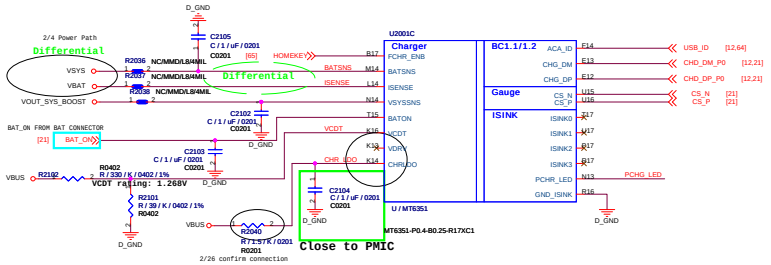
Connect to interface for reserving layout area

DCXO32K_EN	XMODE	CLK OUT
0		0(TCXO on MT6351
1	0	VCTCXO on MT6176
	1	IDFF IO in MT6351
0		1(Tst on MT6351, w/ RTC
1		1(Tst on MT6351, w/o RTC

MEDIATEK

20_POWER_MT6351

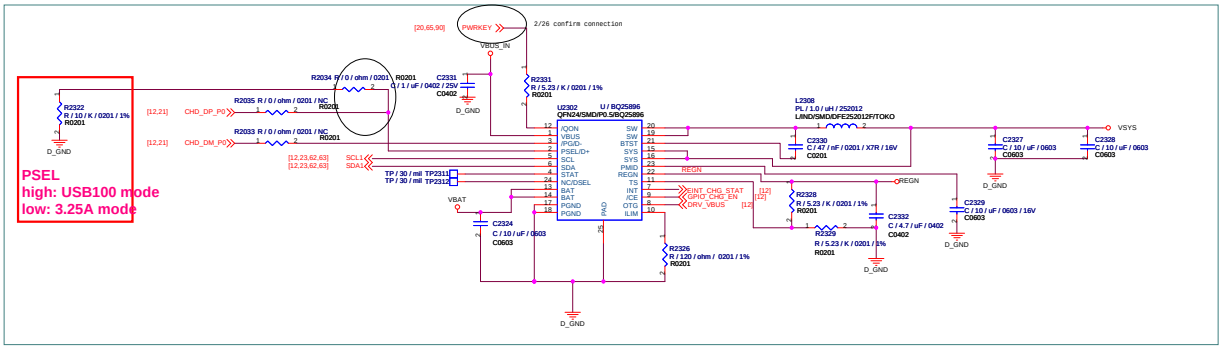
MTK Confidential



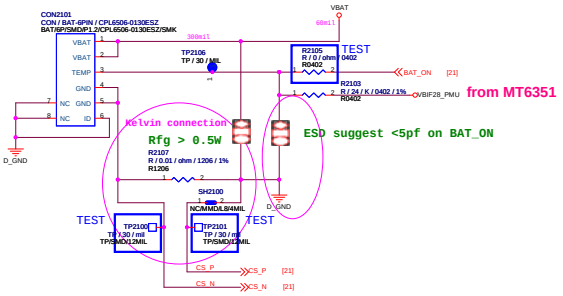
	Internal charger	External charger	
	Pulse charger	Power Path	No Power Path
BATSNS	VBAT	VSYS	VBAT
ISENSE	VBAT(Rsns)	VBAT	VBAT
VSYSNS	VBoost	VBoost	VBoost

Switching Charger + Power Path

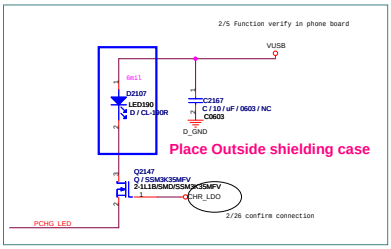
SW CHG + PP I2C address: 0x6B (Write:0xTBC, Read:0xTBC)



BATTERY CONNECTOR



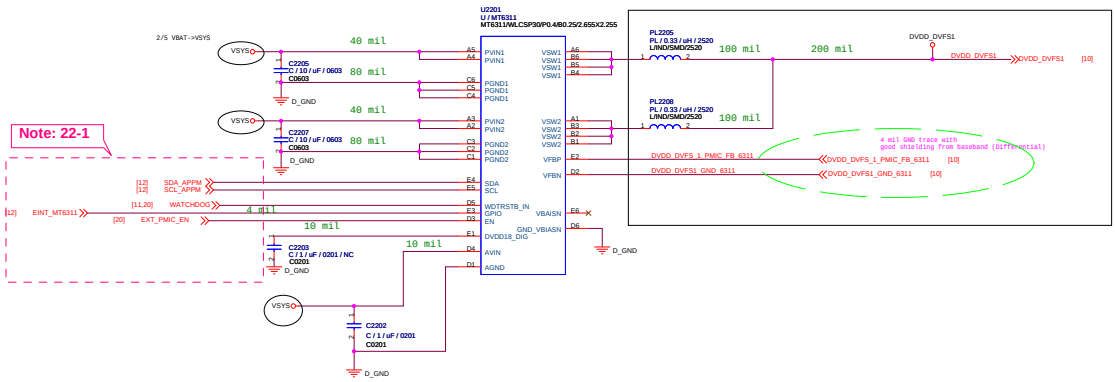
PCHG_LED



File	21_POWER_TBD
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 21 of 99

2-Phase Buck

MT6311 / 2-Phase Buck I2C address: 0X6B (Write:0x, Read:0x)

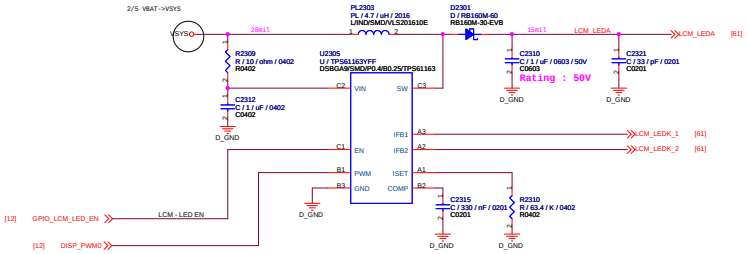


Schematic design notice of "22_POWER_MT6311" page.

Note 22-1: **MT6311 => Buck EN controlled by EXT_PMIC_EN from MT6325 and I2C.**

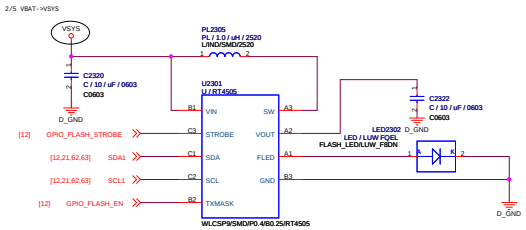
Title	22_POWER_MT6311
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 22 of 99

LCM Backlight LED Driver



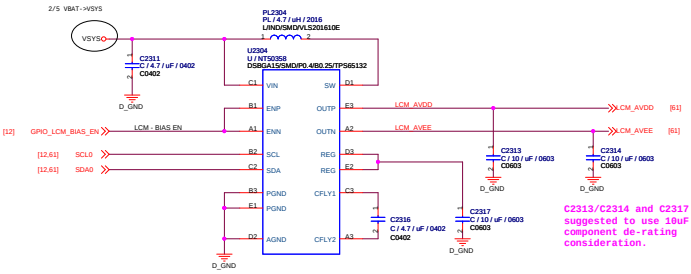
Flash LED 5V Boost

Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)



LCM Gate Drive

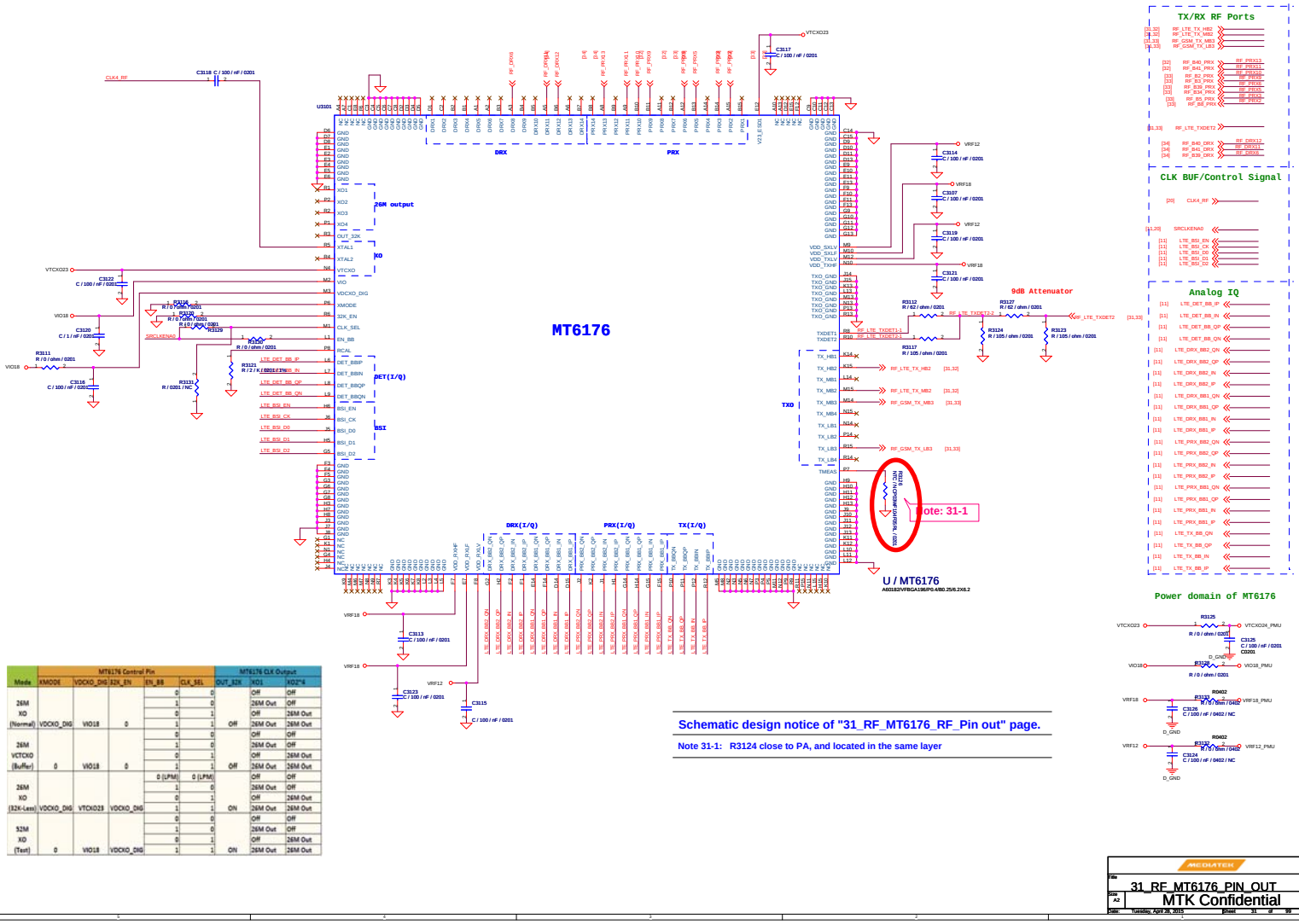
LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)



C2313/C2314 and C2317 are suggested to use 10uF for component de-rating consideration.

MEDIATEK

Title	23_POWER_THIRD-PARTY
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 23 of 99

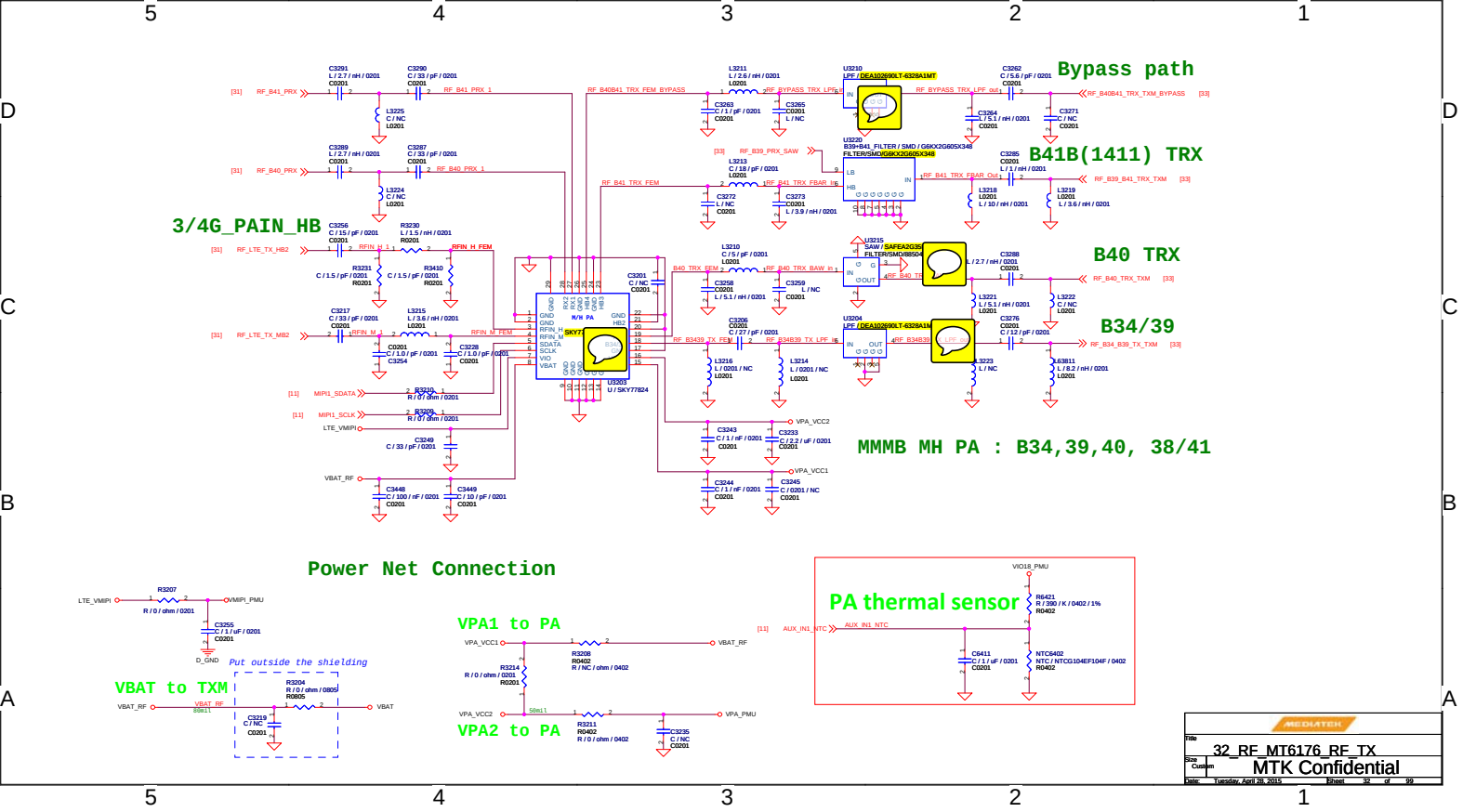


Mode	MT6176 Control Pin					MT6176 CLK Output		
	XMODE	VDCXO_DIG	32K_EN	EN_BB	CLK_SEL	OUT_32K	XO1	XO2*4
26M XO (Normal)	VDCXO_DIG	VIO18	0	0	0	Off	Off	Off
				1	0		26M Out	Off
				0	1		Off	26M Out
				1	1	Off	26M Out	26M Out
26M VCTCXO (Buffer)	0	VIO18	0	0	0	Off	Off	Off
				1	0		26M Out	Off
				0	1		Off	26M Out
				1	1	Off	26M Out	26M Out
26M XO (32K-Less)	VDCXO_DIG	VTCXO23	VDCXO_DIG	0 (LPM)	0 (LPM)		Off	Off
				1	0		26M Out	Off
				0	1		Off	26M Out
				1	1	ON	26M Out	26M Out
52M XO (Test)	0	VIO18	VDCXO_DIG	0	0		Off	Off
				1	0		26M Out	Off
				0	1		Off	26M Out
				1	1	ON	26M Out	26M Out

Schematic design notice of "31_RF_MT6176_RF_Pin out" page.

Note 31-1: R3124 close to PA, and located in the same layer

File	31_RF_MT6176_PIN_OUT
Size	A2
	MTK Confidential
Date:	Tuesday, April 28, 2015
Sheet	31 of 99



Power Net Connection

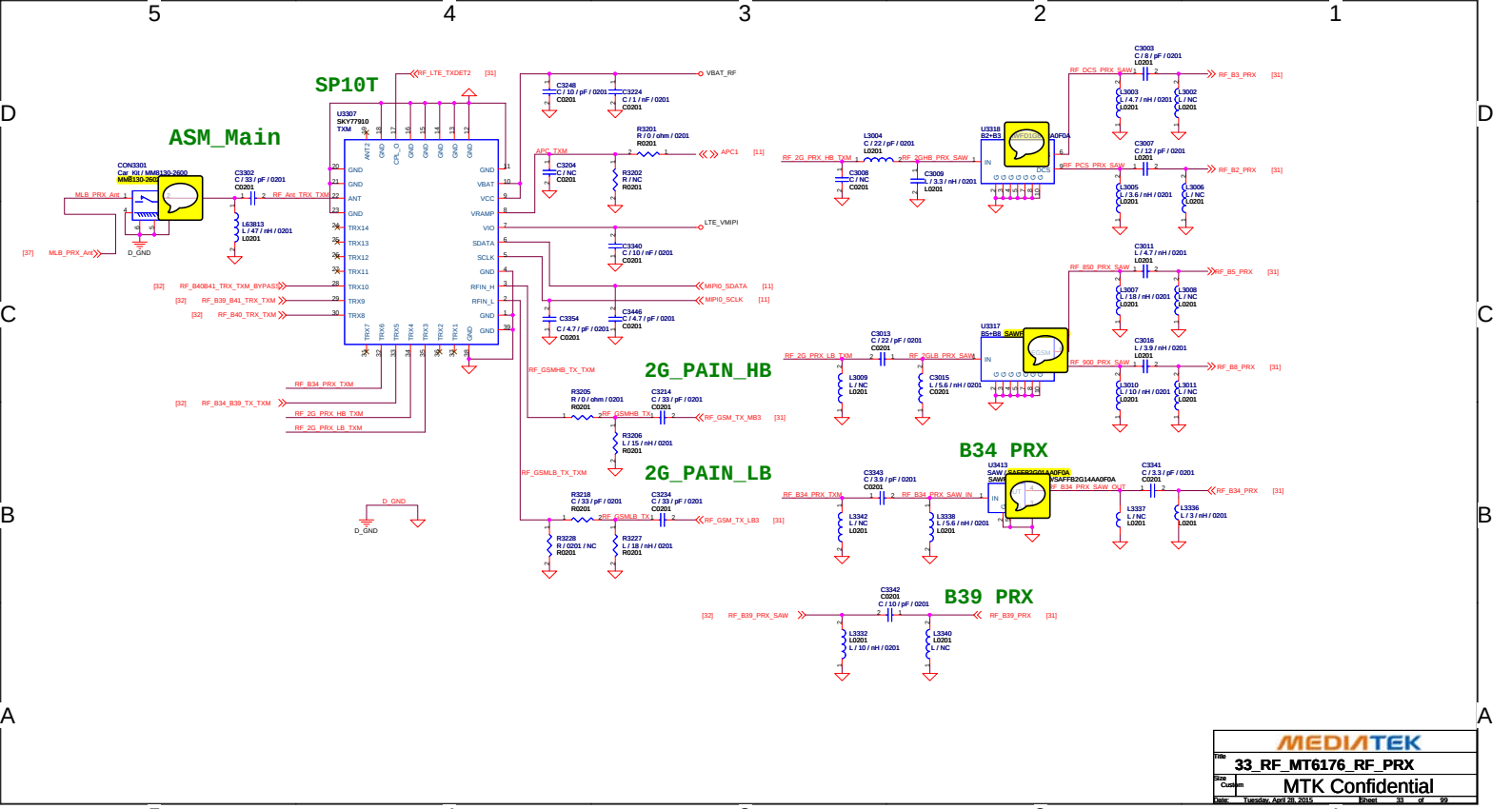
VBAT to TXM

VPA1 to PA

VPA2 to PA

PA thermal sensor

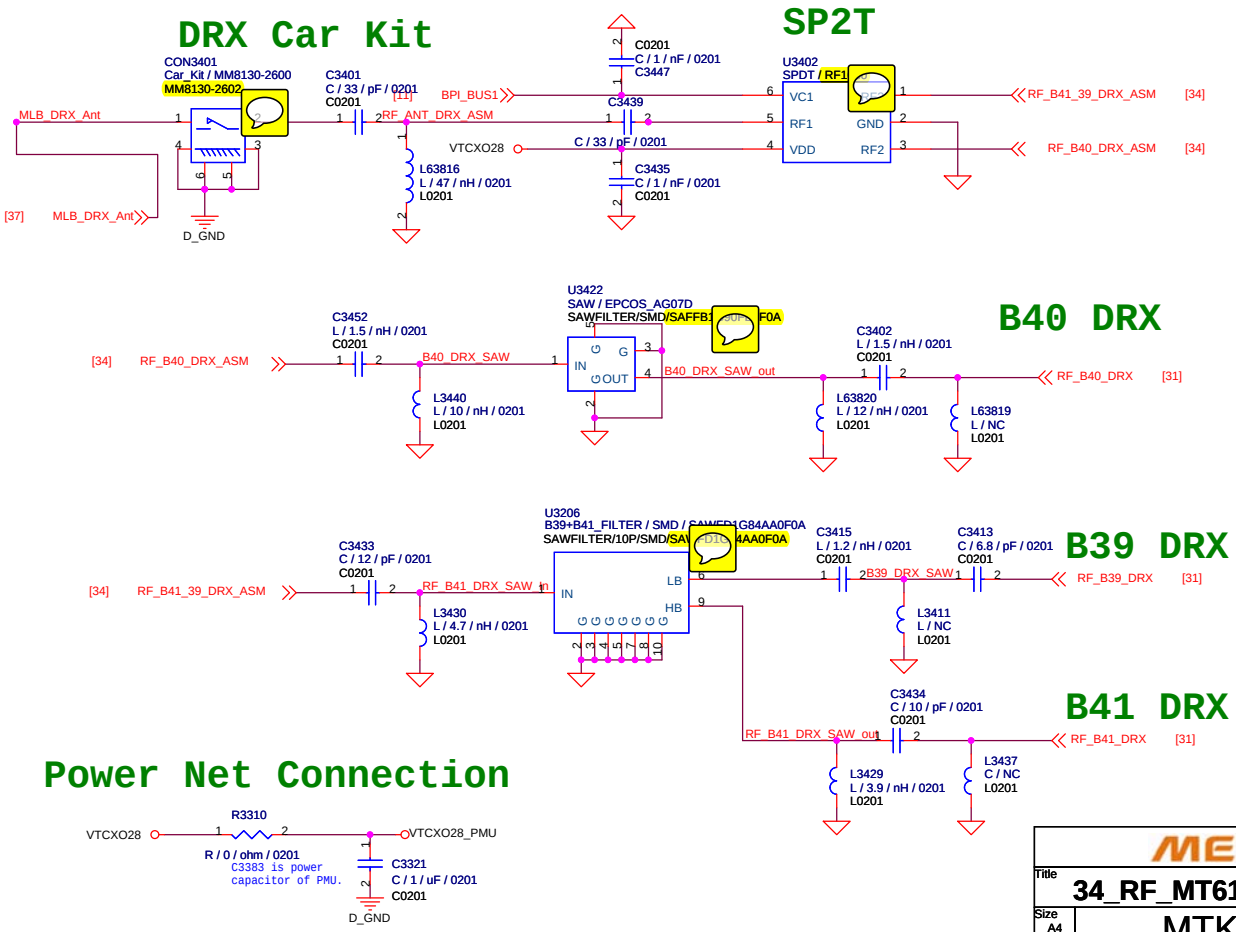
Title	32_RF_MT6176_RF_TX
Size	Custom
	MTK Confidential
Date:	Tuesday, April 28, 2015
Sheet	32 of 99



MEDIATEK

Title	33_RF_MT6176_RF_PRX
Size	Custom
	MTK Confidential
Date:	Tuesday, April 28, 2015
Sheet	33 of 99

DRX ANT: 1805-2690MHz



MEDIATEK

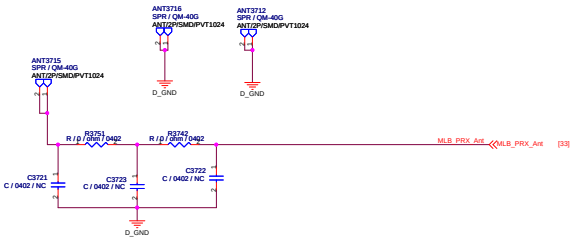
Title: 34_RF_MT6176_RF_DRX

Size: A4

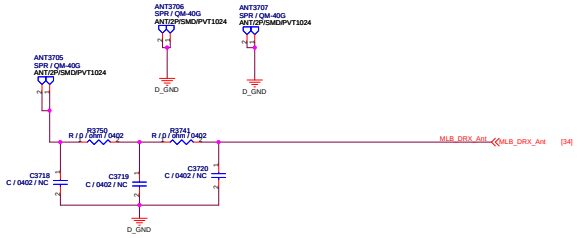
MTK Confidential

Date: Tuesday, April 28, 2015 Sheet 34 of 99

MAIN ANT (ANT0)



RXD ANT (ANT1)



MEDIATEK

Title	37_RF_ANT
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 37 of 99

Off-Page Connector

(To BB IC part)

[11,31] LTE_DET_BB_IP
[11,31] LTE_DET_BB_IN
[11,31] LTE_DET_BB_QP
[11,31] LTE_DET_BB_QN
[11,31] LTE_DRX_BB2_QN
[11,31] LTE_DRX_BB2_QP
[11,31] LTE_DRX_BB2_IN
[11,31] LTE_DRX_BB2_IP
[11,31] LTE_DRX_BB1_QN
[11,31] LTE_DRX_BB1_QP
[11,31] LTE_DRX_BB1_IN
[11,31] LTE_DRX_BB1_IP
[11,31] LTE_PRX_BB2_QN
[11,31] LTE_PRX_BB2_QP
[11,31] LTE_PRX_BB2_IN
[11,31] LTE_PRX_BB2_IP
[11,31] LTE_PRX_BB1_QN
[11,31] LTE_PRX_BB1_QP
[11,31] LTE_PRX_BB1_IN
[11,31] LTE_PRX_BB1_IP
[11,31] LTE_TX_BB_QN
[11,31] LTE_TX_BB_QP
[11,31] LTE_TX_BB_IN
[11,31] LTE_TX_BB_IP

[20,31] CLK4_RF

[11,20,31] SRCLKENA0

[11,31] LTE_BSI_EN
[11,31] LTE_BSI_CK
[11,31] LTE_BSI_D0
[11,31] LTE_BSI_D1
[11,31] LTE_BSI_D2

Off-Page Connector

MIPI0_SDATA [11,33]
MIPI0_SCLK [11,33]

[11,33,38] APC1

[11,33,38] APC1

60mil VBAT
VPA_PMU VPA_PMU
VIO18_PMU
VRF12_PMU
VRF18_PMU
VMIPI_PMU
VTCXO24_PMU
VTCXO28_PMU

MEDIATEK

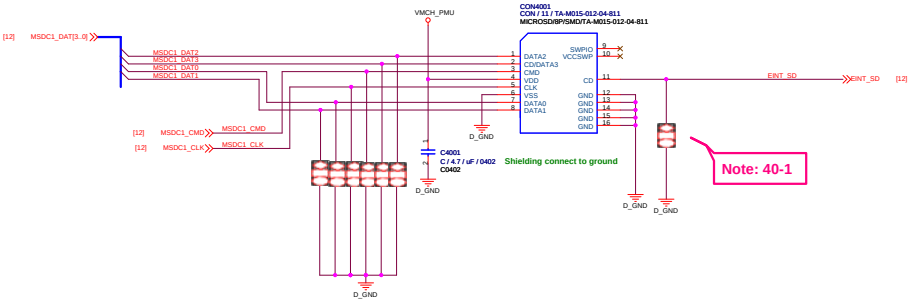
Title: 38_RF Off Page

Size: C

MTK Confidential

Date: Tuesday, April 28, 2015 Sheet 38 of 6

SD CARD



Schematic design notice of "40_MEMORY_SD Card" page.

Note 40-1: The equivalent capacitance of ESD protection device must be <=0.5pF -- otherwise it will result in NFC card mode function fail.

File	40_Memory SD Card
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 40 of 99

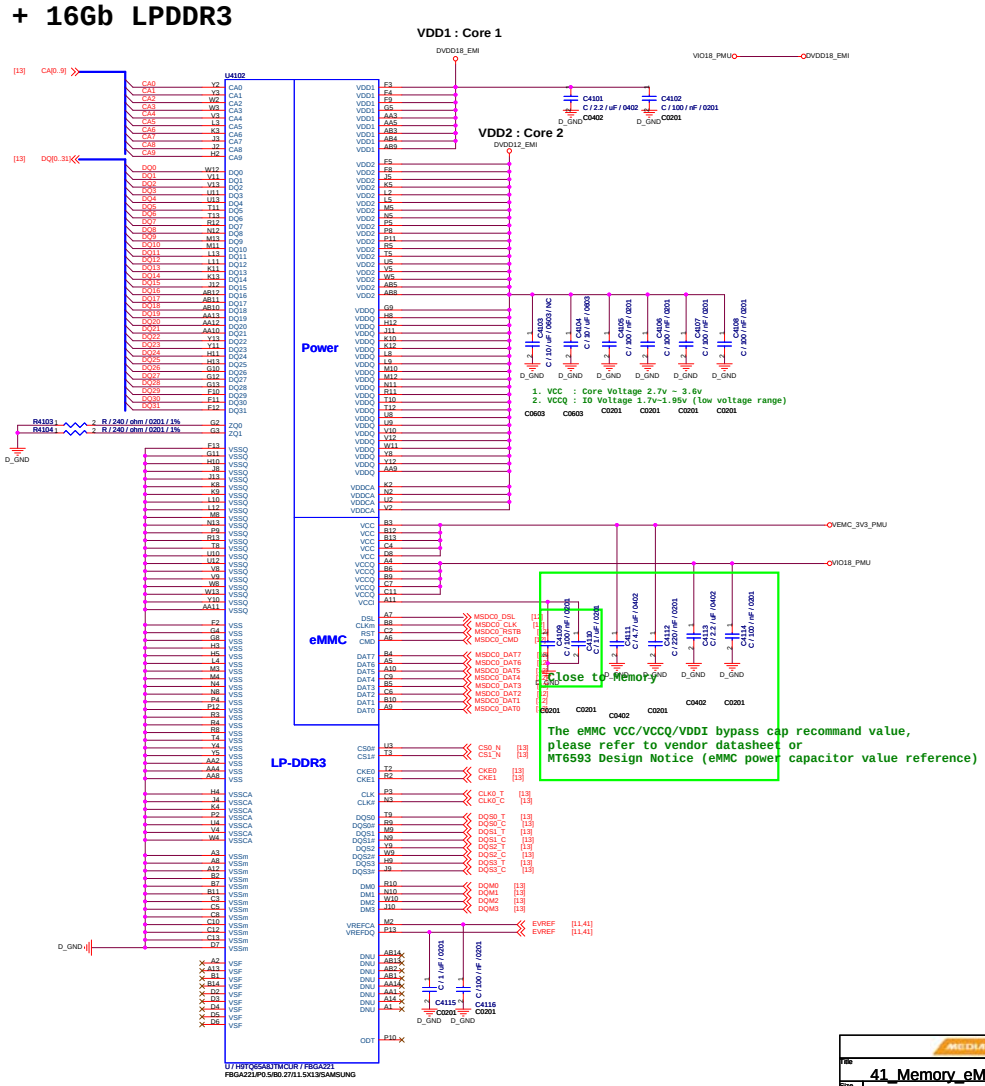
eMMC+LPDDR3　16GB eMMC + 16Gb LPDDR3

221 Ball, 0.5mm pitch

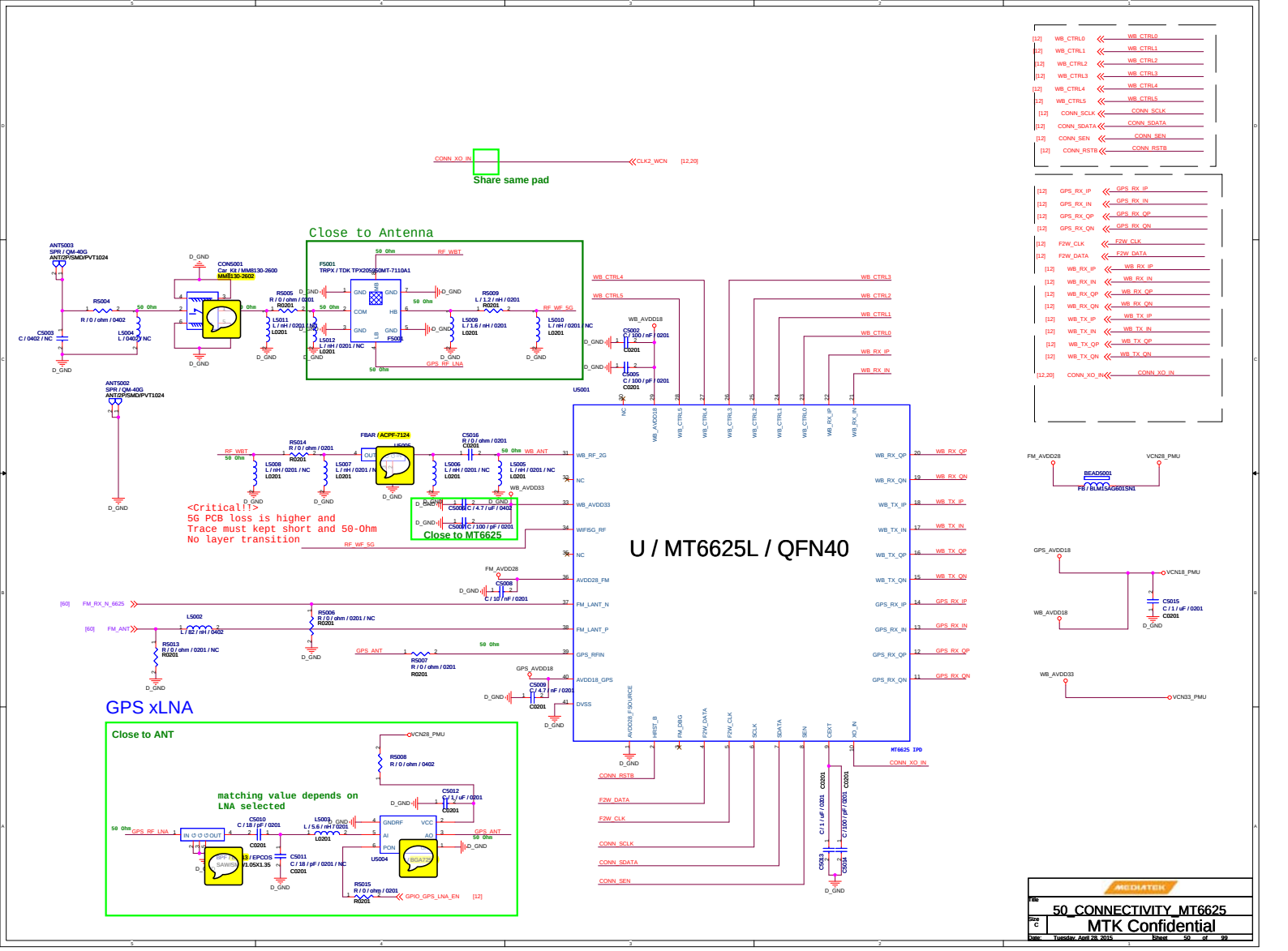
VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V

Connect to AP	
DQ[0..31]	DQ[0..31]
CA[0..9]	CA[0..9]
CS0_N	CS0_N
CS1_N	CS1_N
CKE	CKE
DQM0	DQM0
DQM1	DQM1
DQM2	DQM2
DQM3	DQM3
DQS0_C	DQS0_C
DQS1_C	DQS1_C
DQS2_C	DQS2_C
DQS3_C	DQS3_C
DQS0_T	DQS0_T
DQS1_T	DQS1_T
DQS2_T	DQS2_T
DQS3_T	DQS3_T
CLK0_T	CLK0_T
CLK0_C	CLK0_C
VREF_CA	VREF_CA
VREF_DQ	VREF_DQ
MSDC0_RSTB	MSDC0_RSTB
MSDC0_CMD	MSDC0_CMD
MSDC0_CLK	MSDC0_CLK
MSDC0_DSL	MSDC0_DSL
MSDC0_DAT0	MSDC0_DAT0
MSDC0_DAT1	MSDC0_DAT1
MSDC0_DAT2	MSDC0_DAT2
MSDC0_DAT3	MSDC0_DAT3
MSDC0_DAT4	MSDC0_DAT4
MSDC0_DAT5	MSDC0_DAT5
MSDC0_DAT6	MSDC0_DAT6
MSDC0_DAT7	MSDC0_DAT7

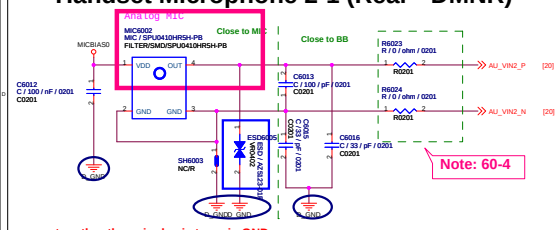
Power I/F	
VIO18_PMU	VIO18_PMU
VEMC_3V3_PMU	VEMC_3V3_PMU
DVDD12_EMI	DVDD12_EMI



File	41_Memory_eMMC_LPDDR3
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 41 of 99

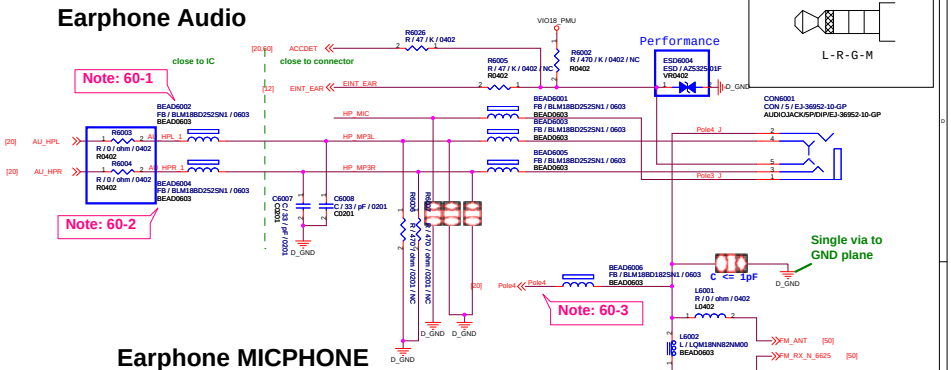

CONN_XO_IN
CLK2_WCN [12,20]
Share same pad
Close to Antenna
ANT5003
SPR / QM-40G
ANT/2P/SMD/PVT1024
CON5001
Cw Kit / MM8130-2600
MM8130-2602
RS004
R / 0 / ohm / 0402
CS003
C / 0402 / NC
LS004
L / 0402 / NC
RS005
R / 0 / ohm / 0201
LS011
L / nH / 0201 / NC
LS012
L / nH / 0201 / NC
FS001
TRFX / TDK TPX205250MT-7110A1
LS009
L / 1.6 / nH / 0201
LS010
L / nH / 0201 / NC
RS009
L / 1.2 / nH / 0201
RF_WF_5G
GPS_RF_LNA
ANT5002
SPR / QM-40G
ANT/2P/SMD/PVT1024
RS014
R / 0 / ohm / 0201
FBAR / ACPF-7124
LS006
L / nH / 0201 / NC
LS005
L / nH / 0201 / NC
CS016
R / 0 / ohm / 0201
WB_ANT
<Critical !>
5G PCB loss is higher and
Trace must kept short and 50-Ohm
No layer transition
Close to MT6625
CS006 C / 4.7 / uF / 0402
CS007 C / 100 / pF / 0201
RF_WF_5G
FM_RX_N_6625 [60]
FM_ANT [60]
LS002
L / 82 / nH / 0402
RS013
R / 0 / ohm / 0201 / NC
RS006
R / 0 / ohm / 0201 / NC
GPS_ANT
RS007
R / 0 / ohm / 0201
CS008 C / 10 / nF / 0201
CS009 C / 4.7 / uF / 0201
GPS xLNA
Close to ANT
matching value depends on
LNA selected
RS008
R / 0 / ohm / 0402
CS012 C / 1 / uF / 0201
CS010 C / 18 / pF / 0201
LS003 L / 5.6 / nH / 0201
CS011 C / 18 / pF / 0201 / NC
US004
RS015
R / 0 / ohm / 0201
GPIO_GPS_LNA_EN [12]
U / MT6625L / QFN40
WB_CTRL4
WB_CTRL5
WB_AVDD18
CS002 100 / nF / 0201
CS005 C / 100 / pF / 0201
US001
WB_CTRL3
WB_CTRL2
WB_CTRL1
WB_CTRL0
WB_RX_IP
WB_RX_IN
WB_RF_2G
NC
WB_AVDD33
WIFI5G_RF
AVDD28_FM
FM_LANT_N
FM_LANT_P
GPS_RFIN
AVDD18_GPS
DVSS
WB_RX_QP
WB_RX_QN
WB_TX_IP
WB_TX_IN
WB_TX_QP
WB_TX_QN
GPS_RX_IP
GPS_RX_IN
GPS_RX_QP
GPS_RX_QN
AVDD28_FSOURCE
HRST_B
FM_GRG
F2W_DATA
F2W_CLK
SCLK
SDATA
SEN
CERT
XO_IN
MT6625 IPD
CONN_XO_IN
CONN_RSTB
F2W_DATA
F2W_CLK
CONN_SCLK
CONN_SDATA
CONN_SEN
C / 1 / uF / 0201
C / 1000 / pF / 0201
CS013
CS014
FM_AVDD28
VCN28_PMU
BEAD5001
FB / BLM15AG601SN1
GPS_AVDD18
VCN18_PMU
CS015 C / 1 / uF / 0201
WB_AVDD18
WB_AVDD33
VCN33_PMU
[12] WB_CTRL0
[12] WB_CTRL1
[12] WB_CTRL2
[12] WB_CTRL3
[12] WB_CTRL4
[12] WB_CTRL5
[12] CONN_SCLK
[12] CONN_SDATA
[12] CONN_SEN
[12] CONN_RSTB
[12] GPS_RX_IP
[12] GPS_RX_IN
[12] GPS_RX_QP
[12] GPS_RX_QN
[12] F2W_CLK
[12] F2W_DATA
[12] WB_RX_IP
[12] WB_RX_IN
[12] WB_RX_QP
[12] WB_RX_QN
[12] WB_TX_IP
[12] WB_TX_IN
[12] WB_TX_QP
[12] WB_TX_QN
[12,20] CONN_XO_IN
MEDIATEK
50_CONNECTIVITY_MT6625
MTK Confidential
Tuesday, April 28, 2015
Sheet 50 of 99

Handset Microphone 2-1 (Rear - DMNR)

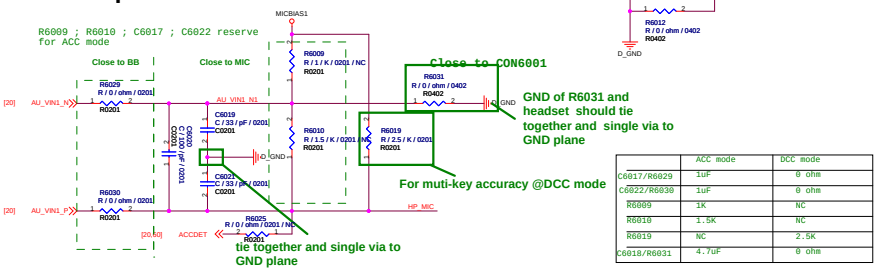


together then single via to main GND

Earphone Audio

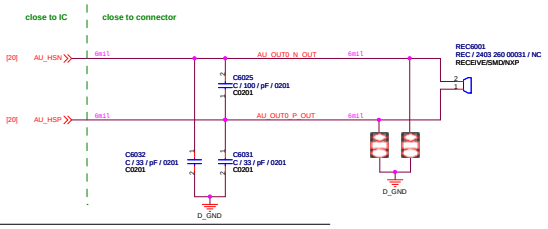


Earphone MICPHONE

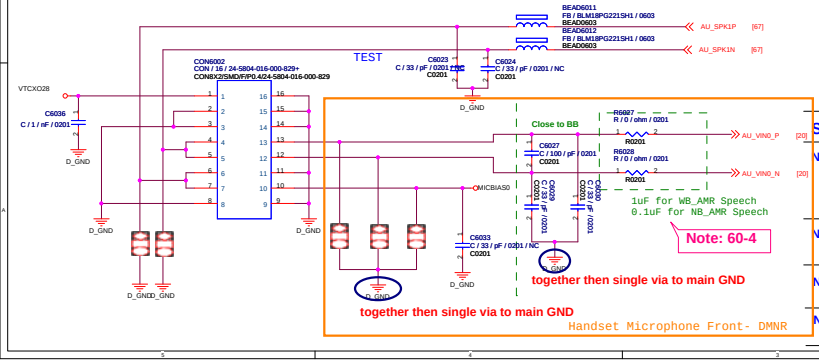


	ACC mode	DCC mode
C6017/R6029	1uF	0 ohm
C6022/R6030	1uF	0 ohm
R6009	1K	NC
R6010	1.5K	NC
R6019	NC	2.5K
C6018/R6031	4.7uF	0 ohm

Receiver



Audio/Speech DTB I/F



Schematic design notice of "60_PERI_AUDIO_IO" page.

Note 60-1: Part # of BEAD6002, BEAD6003, BEAD6004 and BEAD6005 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 60-2: To reserve a resistor in HPL and HPR in series connection both in order to optimize headphone pop noise. The recommended value of this resistor is 33R.

Note 60-3: Layout trace from MT6351 ball G4 AUDREFN to Audio jack GND must surround shield with GND

Note 60-4: 0.1/1 uF for ACC mode (1uF for WB_AMR Speech/0.1uF for NB_AMR Speech) 0 ohm for DCC mode

MEDIATEK

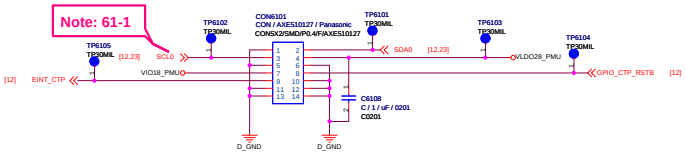
Title: 60_PERI_AUDIO_IO

Size: C

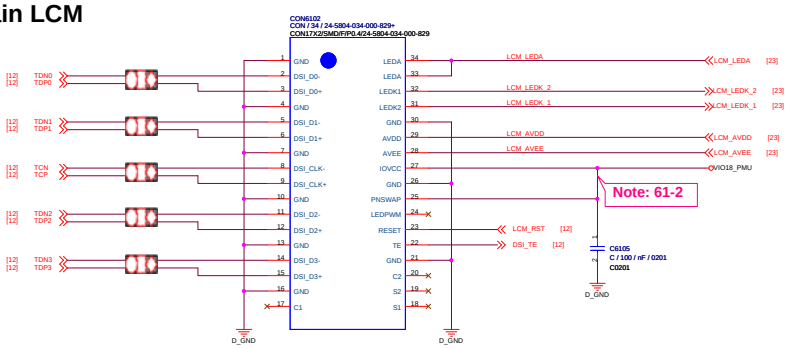
MTK Confidential

Date: Tuesday, April 28, 2015 Sheet 60 of 99

CTP



Main LCM



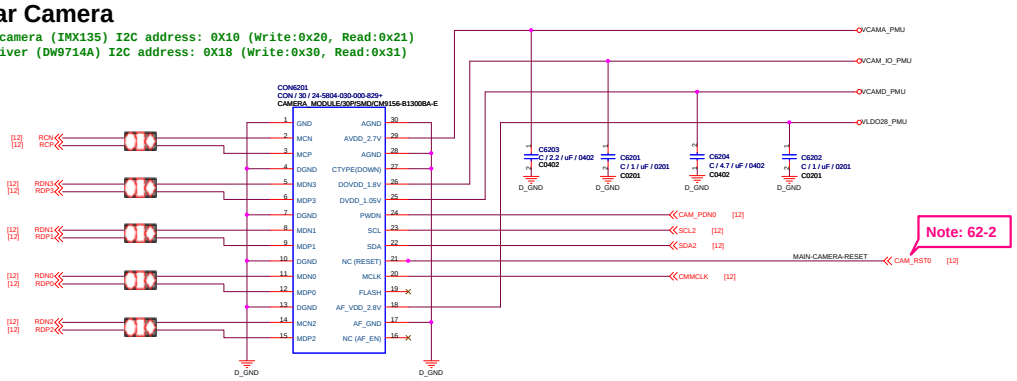
Schematic design notice of "61_PERI_LCD_CTP" page.

Note 61-1: GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB)
or 0x14 (Write:0x28, Read:0x29)

Note 61-2: PNSWAP are used for the polarity swap of MIPI.
PNSWAP=IOVCC => DP=DP,DN=DN;

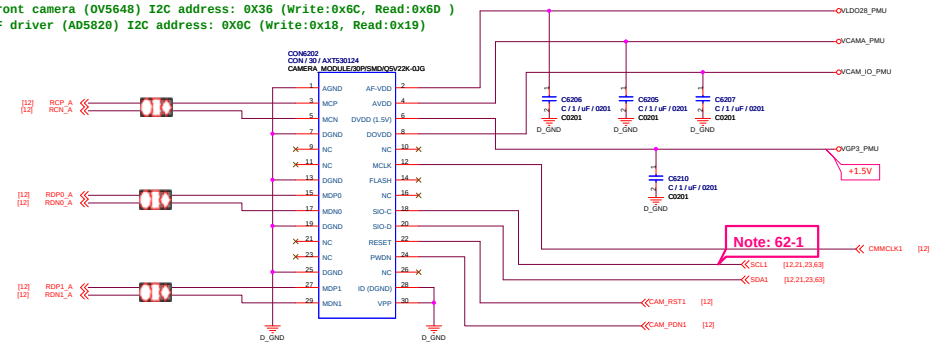
Rear Camera

Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21)
AF driver (DW9714A) I2C address: 0X18 (Write:0x30, Read:0x31)



Front Camera

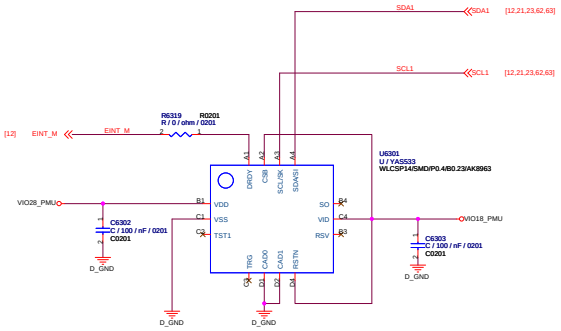
Front camera (OV5648) I2C address: 0X36 (Write:0x6C, Read:0x6D)
AF driver (AD5820) I2C address: 0X0C (Write:0x18, Read:0x19)



Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.
Note 62-1: The VCC of I2C_1/2 is pulled to "VIO18_PMU".
Note 62-2: 16M Camera sensor will pull this PIN to GND, (13M is NC)

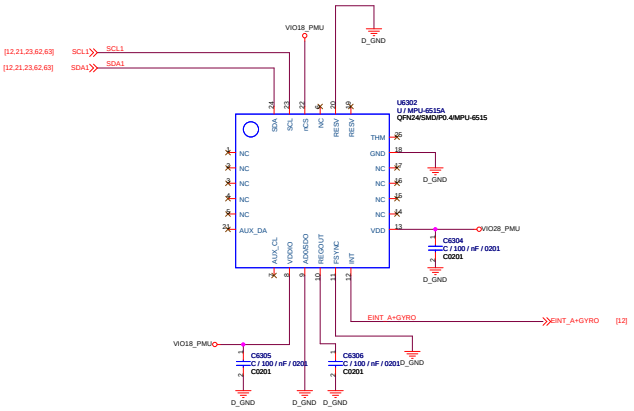
M-Sensor

M-Sensor I2C Address 0x2E (Write: 0x5C, Read: 0x5D)



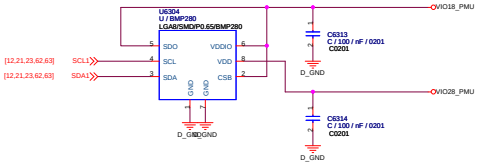
Accerometer + Gyro Sensor

A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)



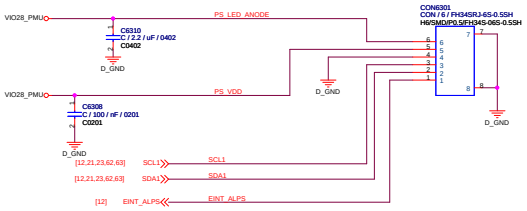
Baro Sensor

Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)

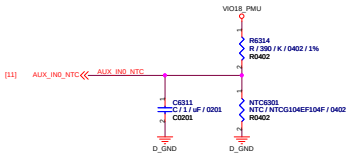


RGB & PS Sensor

CM36558/ RGB+PS I2C address: 0x51 (Write:0x TBC, Read:0xTBC)

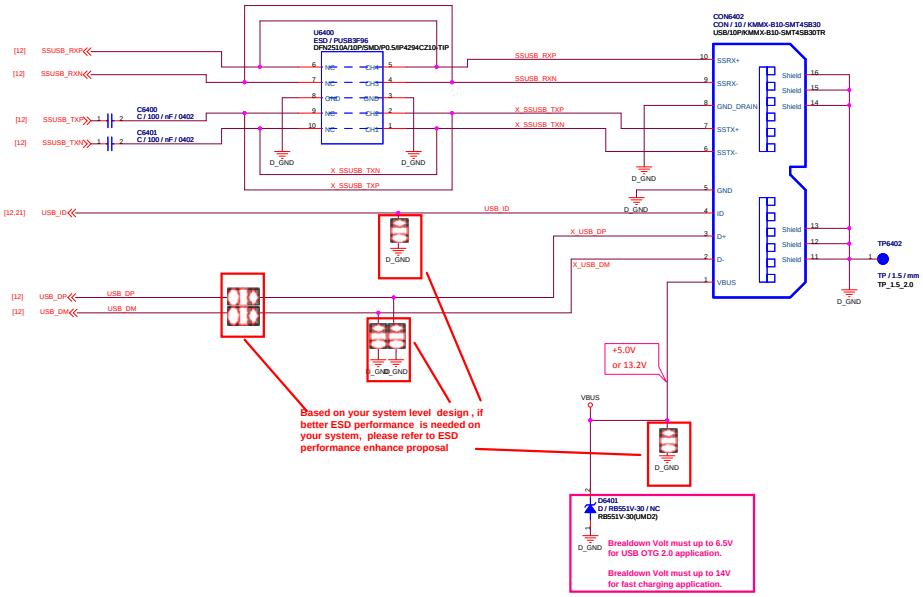


Thermistor / To sense board level temperature



MEDIATEK

Title	63_PERI_SENSORS
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 63 of 99



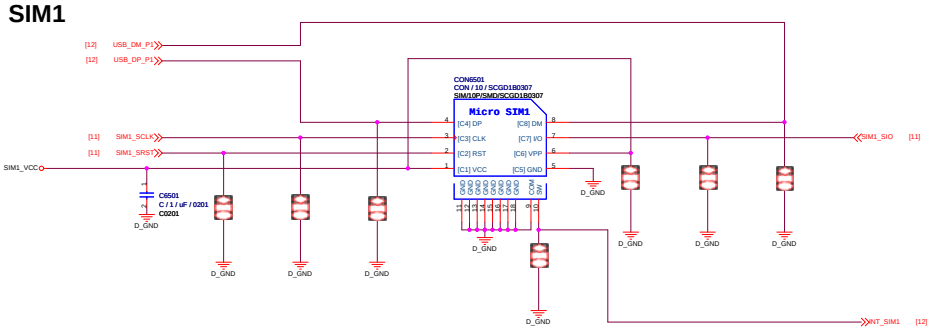
File	64_PERI_USB_MHL
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 64 of 99

SIM POWER I/F

VSIM1_PMU — SIM1_VCC

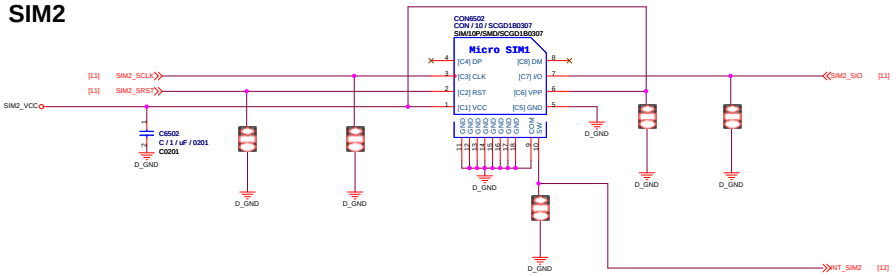
VSIM2_PMU — SIM2_VCC

SIM1



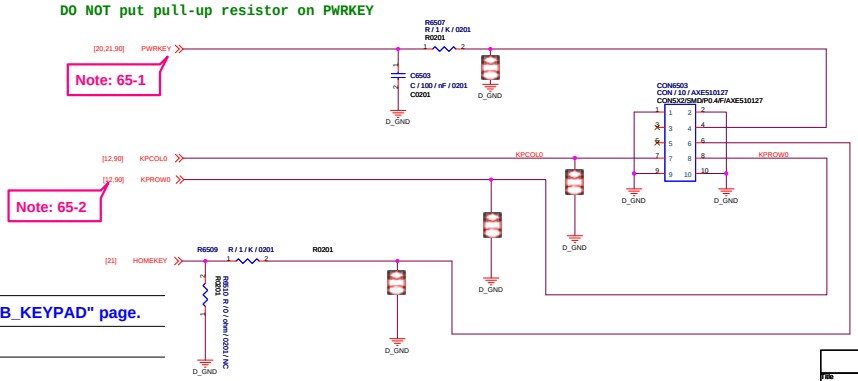
Change part

SIM2



Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 65-1: DO NOT put pull-up resistor on PWRKEY

Note 65-2: Volume Up : HOME Key / GND
Volume Down : KPROW0/KPCOL0

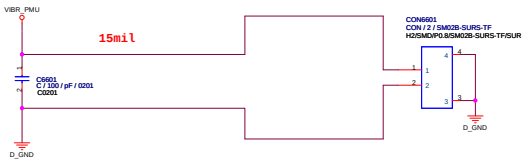
MEDIATEK

File: 65_PERI_Dual_SIM_KEYPAD

Size: C — MTK Confidential

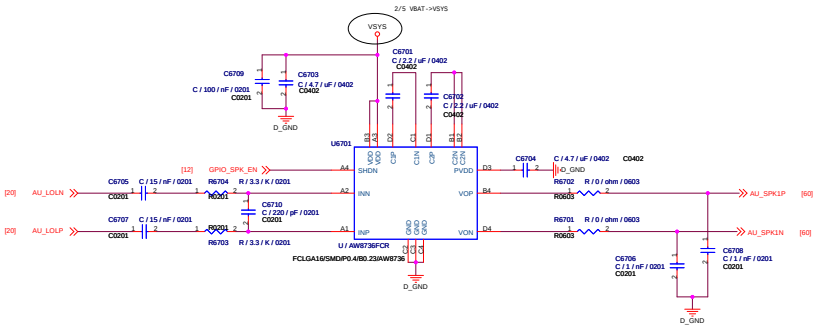
Date: Tuesday, April 28, 2015 Sheet 65 of 99

VIBRATOR



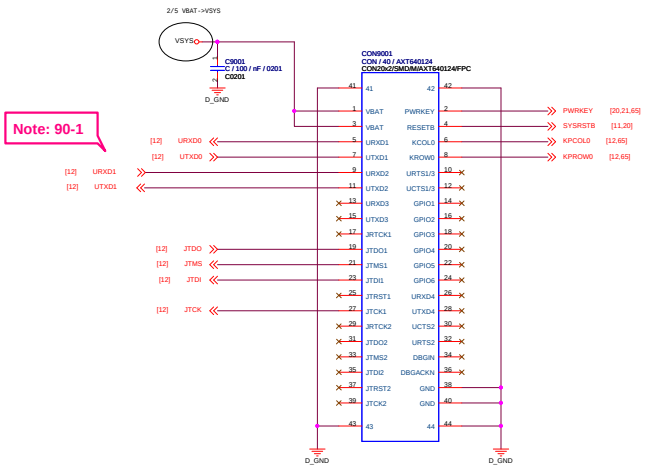
MEDIATEK

File	66_PERI_VIBRATOR
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 66 of 99



MEDIATEK

File	67_PERI_SPEAKER_AMP
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 67 of 99



MEDIATEK

File	90_DEBUG_IO
Size C	MTK Confidential
Date: Tuesday, April 28, 2015	Sheet 90 of 99