MT6311 PMIC Datasheet

Version: 1.0
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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2014-05-20	Johnson Huang	Initial draft
1.0	2015-02-25	Johnson Huang	Release

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Lists of Tables and Figures

1 Overview

1.1 Features

- 2-phase high efficiency buck converter
  - Max. output current: 8.8 A
  - Auto PWM/PFM and Forced-PWM Operations
  - Auto phase shedding
  - Remote differential feedback voltage sensing
  - Programmable output voltage: 0.6 V to 1.4 V in 6.25 mV steps
- Over-current and thermal overload protection.
- One sink current LDO for enhancement DRAM driver reliability
- Under Voltage Lock-Out (UVLO)
- I2C interface
- 30-pin 2.655 × 2.255 mm WLCSP package.

1.2 Applications

- Smart phones and other portable systems.

1.3 General Descriptions

MT6311 is designed to meet the power management requirements of the latest application processors in mobile phones and similar portable application, containing a 2-phase step-down DC/DC converter and is fully controlled by an I2C-compatible serial interface.

MT6311 focuses on high-efficiency, step-down conversion over a wide output current range. The step-down converter enters a PFM mode at light load and includes automatic phase shedding for maximum efficiency at different current levels. The regulator supports remote differential voltage sensing to compensate I*R drop between the regulator output and the load.

Protection features include current limits, input supply UVLO and temperature shutdown functions.

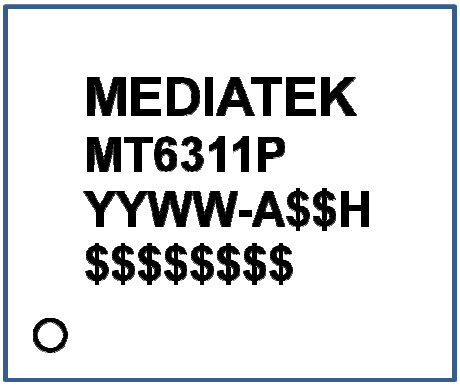
MT6311 is available in a 30-pin WLCSP package. The operating temperature ranges from -25 to +65°C.

1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6311P/A		-25 ~ +65°C	WLCSP 30L

1.5 Top Marking Definition

MT6311P/A



YYWW: Date code
$: Random code

1.6 Pin Assignments and Descriptions

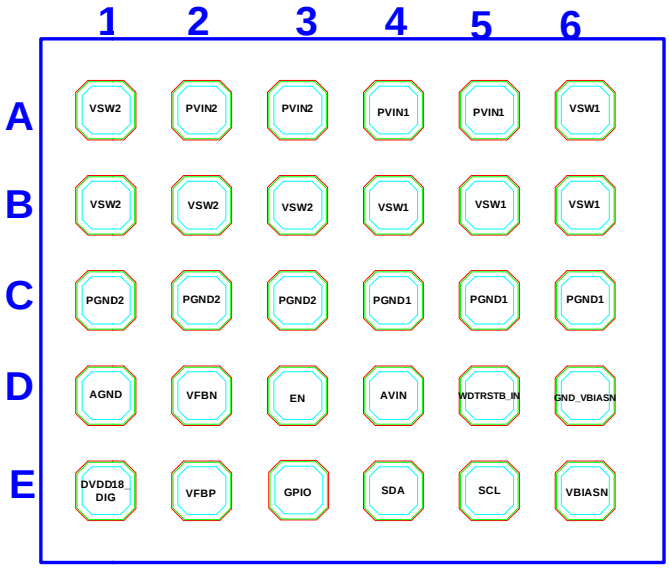


Figure 1-1. MT6311 WLCSP 30 (2.255x2.655mm) pin assignment

Table 1-1. MT6311 pin descriptions

Ball	Symbol	I/O	Description
A6	VSW1	O	SW node of BUCK1
A5	PVIN1	PWR	Power input of BUCK1
A4	PVIN1	PWR	Power input of BUCK1
A3	PVIN2	PWR	Power input of BUCK2
A2	PVIN2	PWR	Power input of BUCK2
A1	VSW2	O	SW node of BUCK2
B6	VSW1	O	SW node of BUCK1
B5	VSW1	O	SW node of BUCK1
B4	VSW1	O	SW node of BUCK1
B3	VSW2	O	SW node of BUCK2
B2	VSW2	O	SW node of BUCK2
B1	VSW2	O	SW node of BUCK2
C6	PGND1	GND	Ground of BUCK1
C5	PGND1	GND	Ground of BUCK1
C4	PGND1	GND	Ground of BUCK1
C3	PGND2	GND	Ground of BUCK2
C2	PGND2	GND	Ground of BUCK2
C1	PGND2	GND	Ground of BUCK2
D6	GND_VBIASN	GND	Ground of VBIASN
D5	WDTRSTB_IN	I	Watchdog reset input signal from AP
D4	AVIN	PWR	Power input of BUCK controller
D3	EN	I	Enable for MT6311
D2	VFBN	I	Feedback of the controller for BUCK1
D1	AGND	GND	Ground of BUCK controller
E6	VBAISN	O	Output node of VBIASN
E5	SCL	I/O	I2C clock
E4	SDA	I/O	I2C data
E3	GPIO	I/O	Interrupt or source clock en pin
E2	VFBP	I	Feedback of the controller for BUCK2 or differential input for BUCK1
E1	DVDD18_DIG	O	Internal digital IO, default floating

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1. Absolute maximum ratings may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery pin input voltage range				5	V
ESD robustness	HBM	2,000			V

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		60.7		°C/W

Note: The device is mounted on a 4-metal-layer PCB (114.3 x 76.2 x 1 mm^3) and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists the operation rang voltages for all MT6311 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A6, B6, B5, B4	VSW1	-0.7~6.2	v
A5, A4	PVIN1	0~5	v
A3,. A2	PVIN2	0~5	v
A1, B3, B2, B1	VSW2	-0.7~6.2	v
C6, C5, C4	PGND1	0	v
C3, C2, C1	PGND2	0	v
E2	VFBP	0~5	v

Ball	Symbol	Voltage range	Unit
D2	VFBN	0~5	v
D6	GND_VBIASN	0	v
D5	WDTRSTB_IN	0~1.98	v
D4	AVIN	0~5	v
D3	EN	0~5	v
D1	AGND	0	v
E6	VBAISN	0~5	v
E5	SCL	0~1.98	v
E4	SDA	0~1.98	v
E3	GPIO	0~1.98	v
E1	DVDD18_DIG	0~1.98	v

2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		65	°C

2.5 Electrical Characteristics

VBAT = 2.6 ~ 4.5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation ground current					
Standby	Low-power mode		55		µA
Under voltage (UV)					
Under voltage ON threshold		2.45	2.5	2.55	V
Under voltage OFF threshold		2.35	2.4	2.45	V
EN					
High voltage		1.5			V
Low voltage				0.63	V
Control input voltage(WDTRSTB_IN, GPIO)					
Control input high		0.7*VIO			V
Control input low				0.3*VIO	V
GPIO					
Output high		VIO-0.4			V
Output low				0.2	V

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal shut-down					
PMIC shut-down threshold			150		degree

2.6 Buck Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VSW1, VSW2					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	VBAT=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	VBAT=3.8V, Vout=0.8V, L_DCR=18mohm I_Load=100mA		80.5		%
	VBAT=3.8V, Vout=1.0V, L_DCR=18mohm I_Load=1000mA		86		%
	VBAT=3.8V, Vout=1.0V, L_DCR=18mohm I_Load=2.0A		87		%
	VBAT=3.8V, Vout=1.0V, L_DCR=18mohm I_Load=5.0A		85		%
Soft start	No load			200	µs
Output Ripple Voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	VBAT=3.8V IOUT = 1.5A to 4A (slew rate=2.5A/us)	-3.5		+3.5	%
DC Accuracy (PWM)	VBAT=2.6V to 4.5V I_Load=20mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.6V to 4.5V I_Load=0~20mA	-2		+3.5	%
Line/Load regulation (PWM)	VBAT= 2.6V to 4.5V I_Load=20mA to Imax	-1		+1	%

2.7 Sink LDO

Table 2-6. Sink LDO specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VBiasN sink current			150		mA
Line/Load regulation	1. VBAT=2.6V to 4.5V	-150		+150	mV

Parameter	Conditions	Min.	Typical	Max.	Unit
	2. TA=-25℃~+65℃ 3. Sink Imax				
Turn-on rise time	1. VBAT=2.6V to 4.5V 2. TA=-25℃~+65℃ 3. Sink Imax			300	us

3 Functional Descriptions

3.1 General Descriptions

MT6311 is a fully integrated PMIC target for smart phone power provider. Figure 3-1. is the block diagram of MT6311 PMIC.

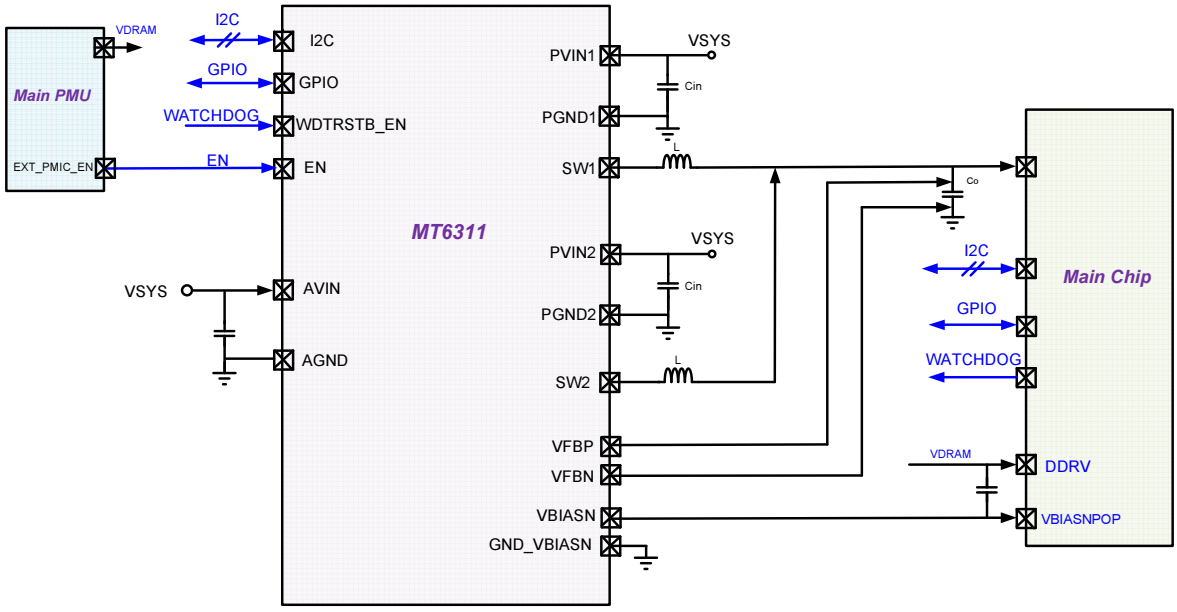


Figure 3-1. MT6311 block diagram

3.2 PMIC Functional Blocks

MT6311 includes the following analog functions for use on smart phone platforms.

- 2-phase BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Sink LDO: One sink current LDO for enhancement DRAM driver reliability

3.2.1 Power-On/Off Sequence

Power-On/Off of the BUCK in MT6311 are controlled by HW pin strapping. The On/Off sequence of VSW controlled by pin “EN” is shown in Figure 3-2 which also depicts that the voltage of VSW will be reduced in sleep mode.

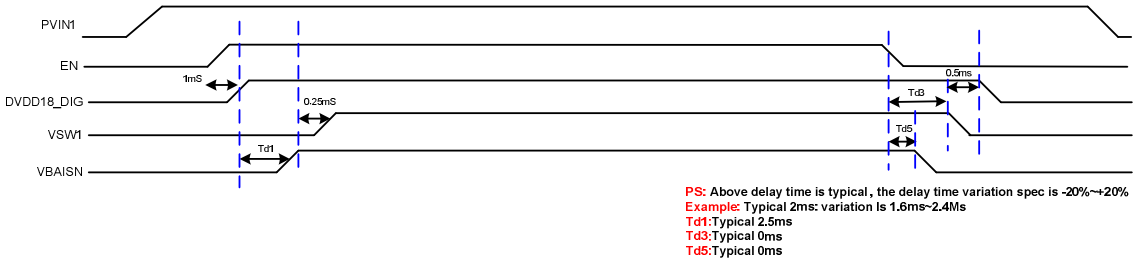


Figure 3-2. Power-on/off control sequence is controlled through pin EN

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are 2-phase buck converters in MT6311 to efficiently generate regulated power for processor. The block diagram is shown in Figure 3-1. The buck converters operate with 3MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

BUCK name	Default Voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VSW	1.0	0.6~1.4	6.25	8800	Y	CPU

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power plan	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
Sink LDO	VBiasN	VBAT	0.30	0.2~0.8	150	Y	Enhancement DRAM driver reliability

3.2.4 Interrupt and Watchdog

3.2.4.1 Interrupt

Interrupt list of PMIC to inform main IC:

1. Buck over current
2. Temperature
   Over 125°C

3.2.4.2 Watchdog

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.5 I2C Interface

MT6311 uses a 2-wire interface consisting of a clock, a chip select and two data signals (SDA and SCL) to connect to main chip. This serial-parallel interface allows main chip to write commands to and read status from PMIC.

3.2.5.1 Data Format

The I2C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between ICs connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a master or slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note that the CLK pin is not used for serial bus data transfer. MT6312 supports standard mode (100kHz), fast mode (400kHz), fast mode plus (1MHz) and high-speed mode (3.4MHz).

3.2.5.2 Protocol

- Slave ID[6:0] = 0x6B
  - Write ID[7:0] = 0xD6 and Read ID[7:0] = 0xD7
- Write time
  - Start (0.5) + ID (9) + Addr (9) + Data (9) + Stop (0.5) + Wait (1) = 29T
- Read time
  - Start (0.5) + ID(9) + Addr (9) + Stop (0.5) + Start (0.5) + ID(9) + Addr (9) + Stop (0.5) + Wait (1) = 39T

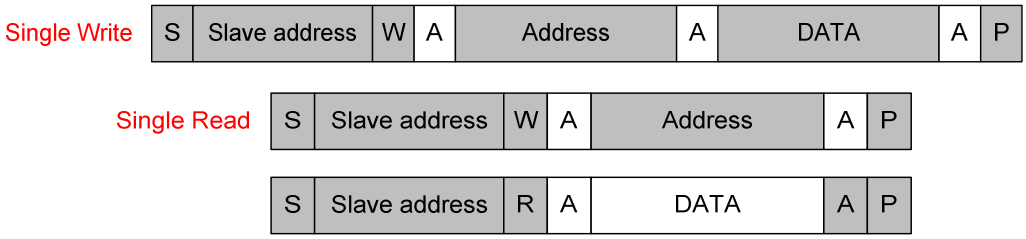


Figure 3-3. I2C single write/read protocol

3.3 Register Table and Descriptions

Module name: PMIC_REG Base address:

Address	Name	Width	Register Function
1C	STRUP_CON2	8	STRUP Control Register 2
28	STRUP_CON14	8	STRUP Control Register 14
66	BUCK_ALL_CON20	8	Buck All Control Register 20
7C	VDVFS1_ANA_CON2	8	VDVFS1 Control Register 2
8D	VDVFS11_CON12	8	VDVFS11 Control Register 12

1C STRUP_CON2 STRUP Control Register 2 00

Bit	7	6	5	4	3	2	1	0
Name	PMU_THR_STATUS							
Type	RO							
Reset	0	0	0					

Bit(s)	Mnemonic	Name	Description
7:5		PMU_THR_STATUS	**Thermal detection status** 3'b000: temperature < 110C 3'b001: temperature > 110C 3'b011: temperature > 125C 3'b111: temperature > 150C

28 STRUP_CON14 STRUP Control Register 14 40

Bit	7	6	5	4	3	2	1	0
Name			RG_STRUP_THR_125_IRQ_STATUS					
Type			RO					
Reset			0					

Bit(s)	Mnemonic	Name	Description
5		RG_STRUP_THR_125_IRQ_STATUS	**Interrupt status condition** 0: None 1: interrupt

66 BUCK_ALL_CON20 Buck All Control Register 20 00

Bit	7	6	5	4	3	2	1	0
Name								VDVFS11_OC_STA

								TUS
Type								RO
Reset								0

Bit(s)	Mnemonic	Name	Description
0		VDVFS11_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs

8D VDVFS11_CON12 VDVFS11 Control Register 12 40

Bit	7	6	5	4	3	2	1	0
Name		VDVFS11_VOSEL						
Type		RW						
Reset		1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0		VDVFS11_VOSEL	**VOUT selection in SW mode** Voltage = 0.6+0.00625*step

4 Application Notes

4.1 Hardware External Shutdown

The figure below shows the configuration for sink LDO that is not used.

- Configuration for sink LDO not in use:
  - Connect GND_VBIASN to GND
  - VBIASN: Floating
  - RG_VBIASN_EN = 0

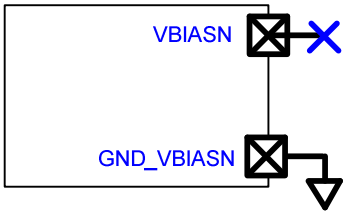
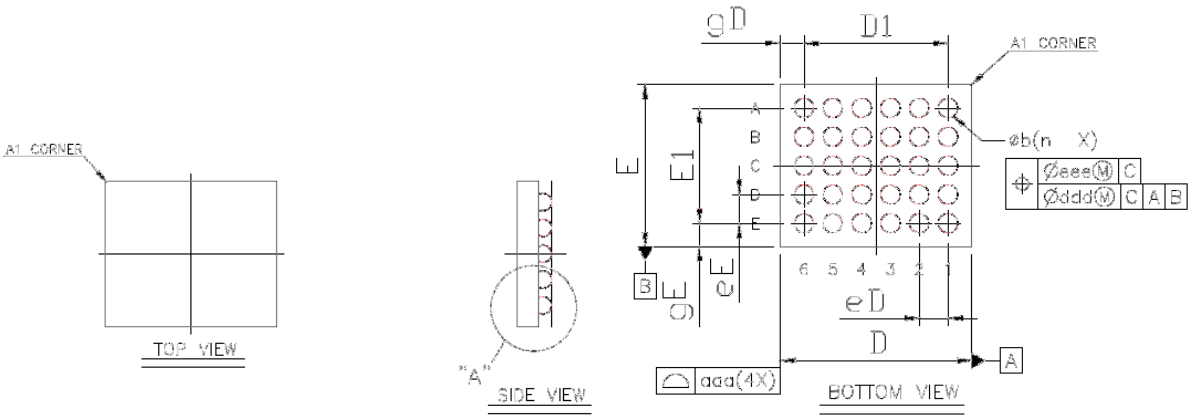


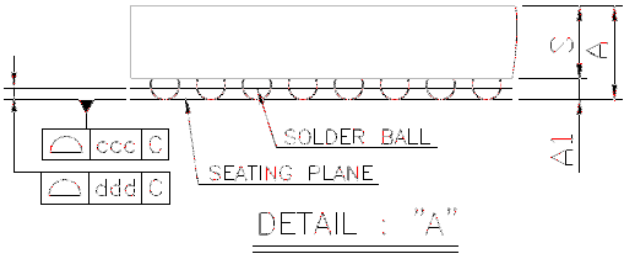
Figure 4-1. Configuration for unused LDO

5 MT6311 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX
Package Type			WLCSP		
Body Size	X	D	2.600	2.655	2.680
	Y	E	2.200	2.255	2.280
Ball Pitch	X	eD	0.400		
	Y	eE	0.400		
Total Thickness		A	0.49	0.53	0.57
Back Side Coating		A2	---		
Wafer Thickness		S	0.305	0.330	0.355
Ball Diameter			0.250		
Stand Off		A1	0.17	0.20	0.23
Ball Width		b	0.24	0.27	0.30
Package Edge Tolerance		aaa	+0.025 −0.055		
Coplanarity		ccc	0.030		
Ball Offset (Package)		ddd	0.050		
Ball Offset (Ball)		eee	0.015		
Ball Count		n	30		
Edge Ball Center to Center	X	D1	2.000		
	Y	E1	1.600		
Edge Ball Center to Package Edge	X	gD	0.3275		
	Y	gE	0.3275		



Appendix