MT6177M RF System

Version: 0.2
Release date: 2017-06-07

Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2017-03-15	Lishin	Initial Template
	2017-03-20	Cyun	Initial Template - RX
	2017-03-22	Calvin	Rx spec
	2017-03-22	Ricky	Update TX specification
0.2	2017-06-07	Lishin	Update TX ball map

Table of Contents

1 Introduction

1.1 Overview

MT6177M is a multi-mode multi-band highly integrated transceiver in 40nm CMOS. This document describes the performance targets for the RF stand-alone chip to be embedded in the overall platform.

1.2 Key Features

- Full multi-mode RF solution (C2K/GGE/WCDMA/TDSCDMA/LTE)
  - Multi-band LTE/WCDMA/TD-SCDMA/GGE/C2K

Band Names					Frequency (MHz)		Support					
LTE	WCDMA	TD-SCDMA	C2K	GSM/EDGE	UL	DL	FDD LTE	TDD LTE	WCDMA	TD-SCDMA	C2K	GSM/EDGE
1	I		BC6		1920-1980	2110-2170	●		●		●	
2	II		BC1	PCS 1900	1850-1910	1930-1990	●		●		●	●
3	III			DCS 1800	1710-1785	1805-1880	●		●			●
4	IV		BC15		1710-1755	2110-2155	●		●		●	
5	V		BC0	GSM 850	824-849	869-894	●		●		●	●
6					830-840	875-885	●					
7					2500-2570	2620-2690	●					
8	VIII			E-GSM 900	880-915	925-960	●		●			●
9	IX				1749.9-1784.9	1844.9-1879.9	●		●			
10					1710-1770	2110-2170	●					
11	XI				1427.9-1447.9	1475.9-1495.9	●		●			
12					699-716	729-746	●					
13					777-787	746-756	●					
14					788-798	758-768	●					
17					704-716	734-746	●					
18			BC10		815-830	860-875	●				●	
19	XIX				830-845	875-890	●		●			
20					832-862	791-821	●					
21					1447.9-1462.9	1495.9-1510.9	●					
22					3410-3490	3510-3590						
23					2000-2020	2180-2200	●					
24					1626.5-1660.5	1525-1559	●					
25					1850-1915	1930-1995	●					
26					814-849	859-894	●					
27					807-824	852-869	●					
28					703-748	758-803	●					
29					N/A	717-728	●					
30					2305-2315	2350-2360	●					
31					452.5-457.5	462.5-467.5						
32					N/A	1452-1496	●					
33					1900-1920	1900-1920		●				
34		a			2010-2025	2010-2025		●		●		
35					1850-1910	1850-1910		●				
36					1930-1990	1930-1990		●				
37					1910-1930	1910-1930		●				
38					2570-2620	2570-2620		●				
39		f			1880-1920	1880-1920		●		●		
40		e			2300-2400	2300-2400		●		●		
41					2496-2690	2496-2690		●				
42					3400-3600	3400-3600						
44					703-803	703-803		●				
45					1447-1467	1447-1467		●				
65					1920-2010	2110-2200	●					
66					1710-1780	2110-2200	●					
67					N/A	738-758	●					
68					698-728	753-783	●					
69					N/A	2570-2620	●					
70					1695-1710	1995-2020	●					
[71]					663-698	617-652	●					

1. DL only

  - 64QAM UL/64QAM DL (HSPA+/LTE)
  - C2K/2G/3G/4G co-banding
  - Supports RxD (10 RxD ports)
  - Supports SRLTE

- Direct Conversion transmitter (LTE/3G/8-PSK) and DFM for GMSK
  - Dedicated power detection circuits for power control over specific power range
  - 2LB/2MB/1HB TX output port
- Hybrid Direct-Conversion (4G/3G/C2K)/Low-IF (GGE, DC-HSDPA) receiver
  - 10+10 Rx input ports
  - 2 RXIF IQ outputs.
- Two SAWless Rx input ports for GGE (B2, B3, B5, and B8), TDSCDMA and TDD LTE (B34 and B39).
- Support external LNA at RxP and RxD.
- Low supply current & operation directly from dual DC-DC converters
- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feed-through, IIP2, DC offset, RC corner)
- Support LTE Power Class 2 high-power UE (HPUE) in band 41

2 Block Diagram and Application Diagram

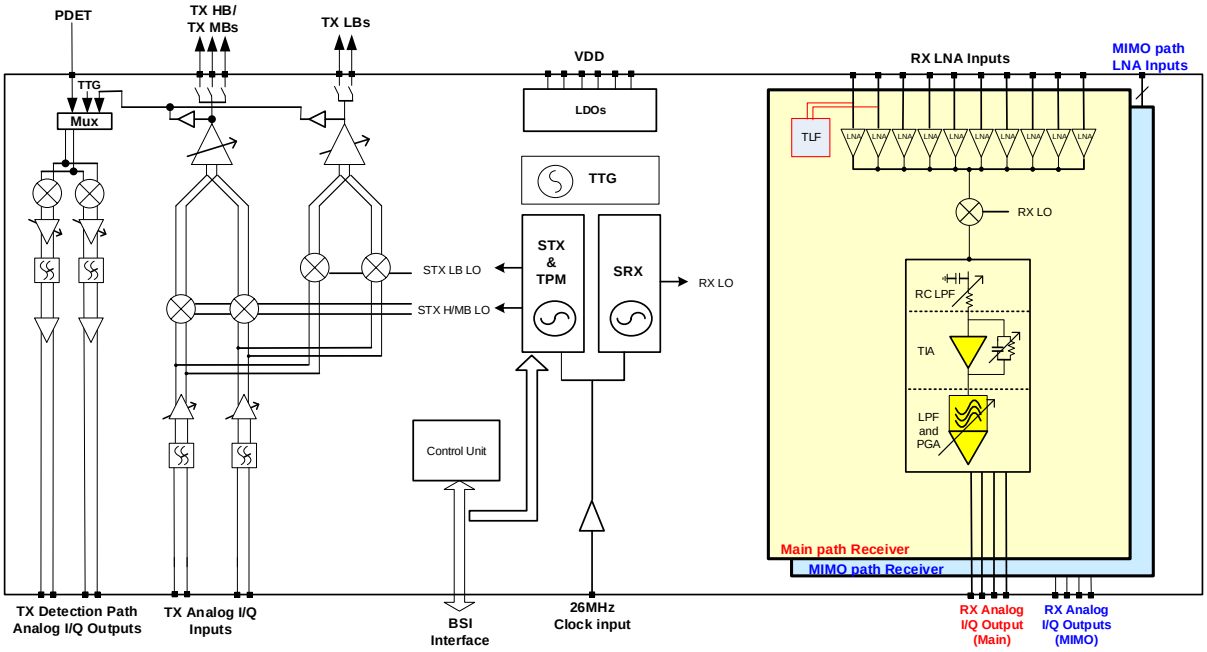
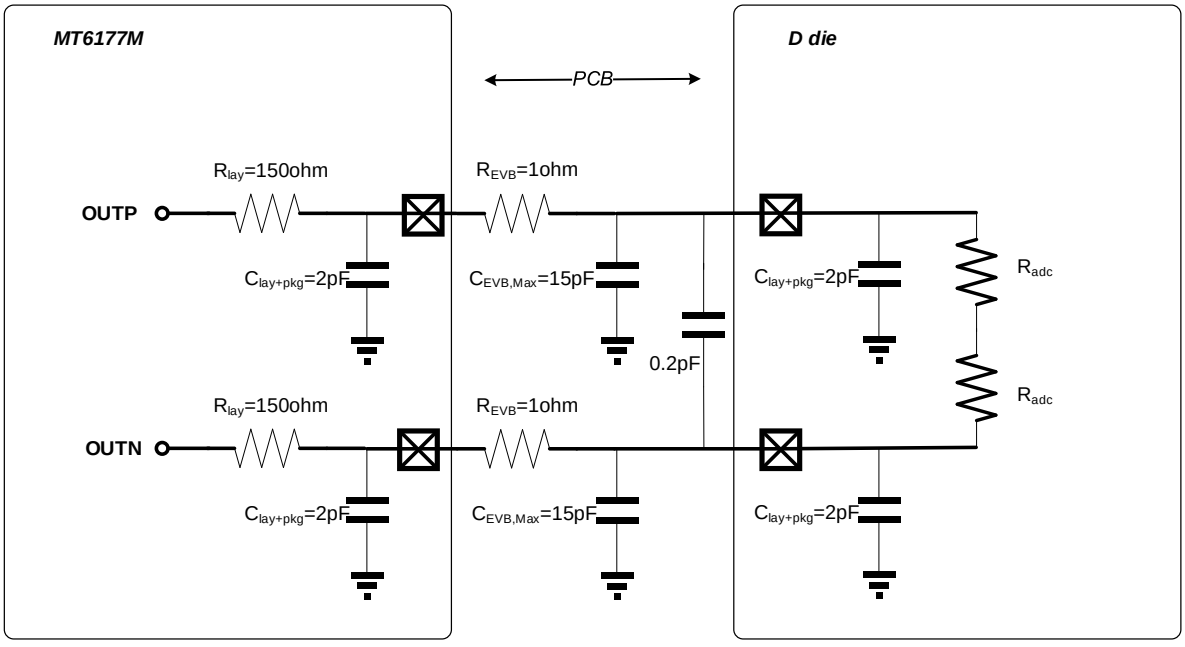


Figure 2-1. RFSYS block diagram

- RXIF IQ output loading model



For the applications whose bandwidth are the maximum of LTE 20MHz, we highly recommend PCB loading should be small enough (<15pF) to avoid extra drooping in band-edge and performance degradation. Inevitably, in some special case the PCB IQ traces may be longer and make PCB loading larger, the value would be up to several tens of pF. In these cases, limited performance can only be achieved. For example, the maximal throughput would be degraded.

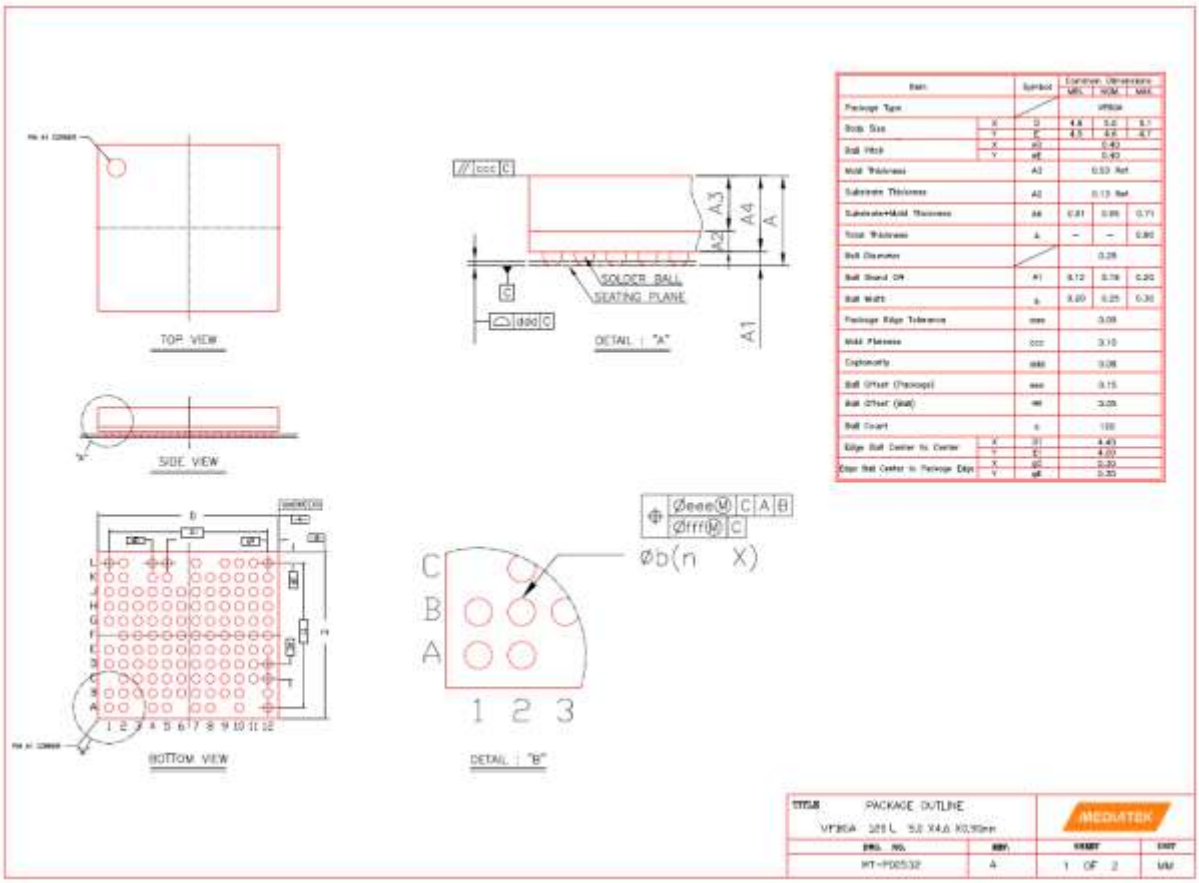
PCB trace requirement of Rx IF interface:

1. Capacitance loading < 15pF
2. Mismatch between capacitance of I path and Q path < 10%
3. The trace to trace isolation has been defined in system application note.
   Should pay attention to the isolation between traces for required performance.

3 General Specifications

3.1 Packaging

Wirebond VFBGA is currently considered for this product.



Parameter	Single die
Body Size (width/length/height)	5.0x4.6x0.9mm
Ball Spacing	0.4mm
Ball array	12x11

3.2 IC Marking

YYWW: date code
#: subcontractor code
$$$$$$$: LOT NO.

3.3 RF I/O List

Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF pin	
RF I/O	SWLB		I	RF	Primary RX SAWless LB
	SWHB		I	RF	Primary RX SAWless HB
	PRX1		I	RF	Primary RX input 1
	PRX2		I	RF	Primary RX input 2
	PRX3		I	RF	Primary RX input 3
	PRX4		I	RF	Primary RX input 4
	PRX5		I	RF	Primary RX input 5
	PRX6		I	RF	Primary RX input 6
	PRX7		I	RF	Primary RX input 7
	PRX8		I	RF	Primary RX input 8
	DRX1		I	RF	Diversity RX input 1
	DRX2		I	RF	Diversity RX input 2
	DRX3		I	RF	Diversity RX input 3
	DRX4		I	RF	Diversity RX input 4
	DRX5		I	RF	Diversity RX input 5
	DRX6		I	RF	Diversity RX input 6
	DRX7		I	RF	Diversity RX input 7
	DRX8		I	RF	Diversity RX input 8
	DRX9		I	RF	Diversity RX input 9
	DRX10		I	RF	Diversity RX input 10
	TXO1		O	RF	TX HB output
	TXO2		O	RF	TX MB1 output
	TXO3		O	RF	TX MB2 output (2G)
	TXO4		O	RF	TX LB1 output (2G)

Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF pin	
	TXO5		O	RF	TX LB2 output
	TXDET1		I	RF	TX detection path input
BB I/O	RX1_BBIP		O	BB	RX1 BB I output
	RX1_BBIN		O	BB	RX1 BB I output
	RX1_BBQP		O	BB	RX1 BB Q output
	RX1_BBQN		O	BB	RX1 BB Q output
	RX2_BBIP		O	BB	RX2 BB I output
	RX2_BBIN		O	BB	RX2 BB I output
	RX2_BBQP		O	BB	RX2 BB Q output
	RX2_BBQN		O	BB	RX2 BB Q output
	TX_BBIP		I	BB	TX BB I input
	TX_BBIN		I	BB	TX BB I input
	TX_BBQP		I	BB	TX BB Q input
	TX_BBQN		I	BB	TX BB Q input
	DET_IP		O	BB	TX detection path I output, test pin 0
	DET_IN		O	BB	TX detection path I output, test pin 1
	DET_QP		O	BB	TX detection path Q output, test pin 2
	DET_QN		O	BB	TX detection path Q output, test pin 3
BSI Interface and CLK Input	BSI_EN		I	GPIO	BSI enable
	BSI_CLK		I	GPIO	BSI clock
	BSI_D0		I/O	GPIO	BSI input/output data
	BSI_D1		I/O	GPIO	BSI input/output data
	BSI_D2		I/O	GPIO	BSI input/output data
	XO_IN		I	RF	26MHz input
	EN_BB		I		Global static controller enable
	RCAL		O	DC	External resistor calibration pin
Voltage Supply	VDD_RXHF		VDD	RF	DCDC 1.8V supply for RX
	VDD_RXLV		VDD	RF	DCDC 1.2V supply for RX
	VDD_TXHF		VDD	RF	DCDC 1.8V supply for TX
	VDD_STXHF		VDD	RF	DCDC 1.8V supply for STX and TX
	VDD_STXLV		VDD	RF	DCDC 1.2V supply for STX
	VIO		VDD	RF	Always on 1.8V for digital
	TXO_GND		GND	RF	TX output ground
	GND		GND	RF	RF ground

3.4 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	
A	DRX2	DRX1		PRX8	PRX6		PRX4	PRX2		TXO4(2G)		TXO3(2G)	A
B	DRX4	DRX3	SWLB	SWHB	PRX7	PRX5	PRX3	PRX1	GND	TX_GND		TX_GND	B
C		DRX5	GND	GND	GND	GND	GND	GND	GND	TX_GND	TXO5	TXO2	C
D	DRX6	DRX7	GND	GND	GND	GND	GND	GND	GND	TX_GND	TX_GND	TXO1	D
E	DRX8	DRX9	VDD_RXLV	GND	GND	GND	GND	GND	GND	GND	GND	GND	E
F		DRX10	GND	GND	GND	GND	GND	GND	GND	STX_MON	GND	VDD_TXHF	F
G	RCAL	VDD_RXHF	GND	EN_BB	GND	GND	GND	GND	GND	GND	GND	GND	G
H	BSI_EN	BSI_D0	GND	GND	GND	GND	GND	GND	GND	GND	GND	TX_BBIP	H
J	BSI_D1	BSI_D2	RX2_BBIP	RX2_BBIN	RX1_BBQN	RX1_BBQP	GND	GND	GND	VDD_STXHF	GND	TX_BBIN	J
K	BSI_CLK	GND		RX2_BBQN	RX1_BBIN		DET_QP	DET_QN	DET_IN	GND	GND	TX_BBQN	K
L	VIO	XO_IN		RX2_BBQP	RX1_BBIP		TXDET1		DET_IP	GND	VDD_STXLV	TX_BBQP	L
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 3-1. Ball map

3.5 Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit	Notes
Supply VIO18		-0.3	2.0	V	
Supply VRF18		-0.3	2.0	V	
Supply VRF12		-0.3	1.3	V	
Junction Temperature			125	°C	
ESD Protection	HBM – analog and digital I/O	≧1000V		V	
	HBM – RF I/O	≧1000V		V	PDET, Rx inputs, Tx outputs
	FICDM – analog and digital I/O	±250		V	target - no current corporate requirement
	FICDM– RF I/O	±250		V	PDET, Rx inputs, Tx outputs target - no current corporate requirement

Notes

1. No DC input should be directly applied to the Rx inputs.
2. Tx output: No DC should be applied under any circumstances (AC coupling required for those PA's with DC at the input).

3.6 Operating Conditions

Within the operating range the IC operates as per the functional description.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Supply VIO18		1.7	1.8	2	V
Supply VRF18		1.75	1.81	2	V
Supply VRF12		1.11	1.2	1.3	V
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	

Note 1
The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB, etc).

Operation/Test condition	PCB temperature (°C)
TTC	+25°
ETC	-30° to +85°

Note 2
The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this.

3.7 BSI Speed

PAD Name	Normal Mode	Normal mode direction	ATPG mode	ATPG mode direction
BSI_CLK	BSI_CLK	I (60MHz)	SCLK	I (100MHz)
BSI_EN	BSI_EN	I (60MHz)	SCAN_ENABLE	I (100MHz)
BSI_DATA0	BSI_DATA0	Bi-directional (60MHz)	SCAN_IN	I (100MHz)
BSI_DATA1	BSI_DATA1	Bi-directional (60MHz)	SCAN_OUT	O (100MHz)
BSI_DATA2	BSI_DATA2	Bi-directional (60MHz)	ATPG_RESETB	I (100MHz)

4 Supply Specification

4.1 External Power Supplies and Interfaces

The RFSYS macro operates from three power supplies.

Supply name	Usage	Regulator type	Output voltage
VRF18	LDO supply (from system DCDC) for all major sub- systems	Linear with ripple	1.81V
VRF12	LDO supply (from system DCDC) for all major sub- systems	Linear with ripple	1.2V
VIO18	LDO supply (from system DCDC) ; Always-on supply for interface and register retention	Linear with ripple	1.8V

5 Transmitter

All transmitter characteristics are listed in this section. Typical specifications are for mid-band channel frequency, and under typical operating conditions. Min/Max specifications are for extreme operating voltage and temperature conditions.

5.1 Tx Block Diagram

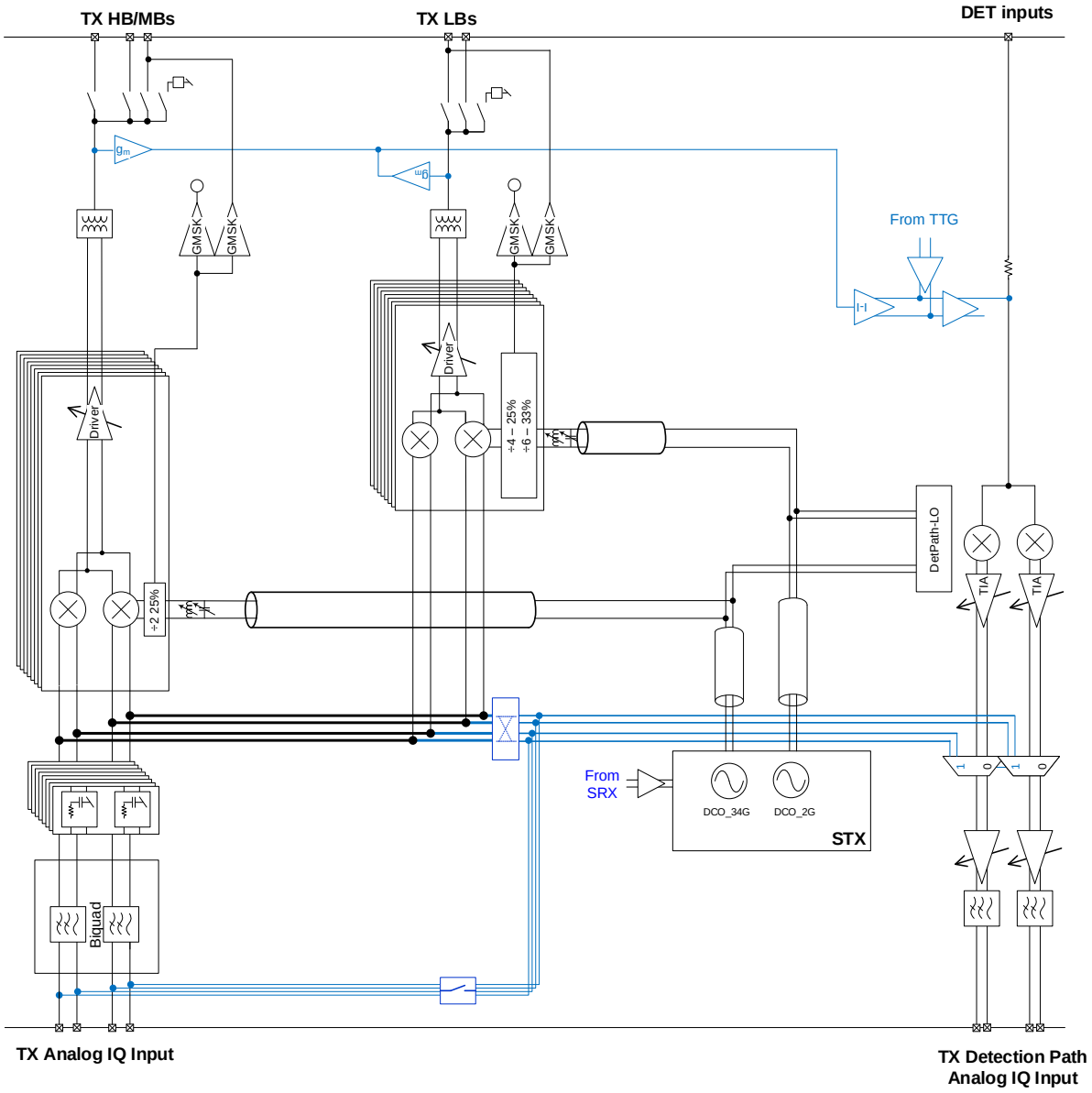


Figure 5-1. Tx block diagram

The transmitter is designed for high performance and low power consumption. It consists of two signal paths: low-band and mid-band/high-band (LB, MB/HB). The two paths share a common analog base-band active low-pass filter and a common passive RC low-pass filter. After that, the I/Q baseband signals are up-converted by one of two fully-differential passive mixers and amplified by the RF driver (PGA). The differential output is converted to single-ended using a balun. Finally the single-ended RF signal is routed to the desired output pin by the output switch. Note that only one TX-path and one output pin switch are active at a time. Singled-ended Tx signals at the output of the two signal paths (LB, MB/HB) are connected together to a common detector path used for calibration.

Each signal path (LB, MB/HB) has its corresponding LO distribution circuitry. The LO distribution design is optimized for low power consumption. The Detector path has a single-ended RF input for high accuracy power control and Digital Predistortion (DPD).

BAND	RATs	Lower edge MHz	Upper edge MHz	TX chain
1	WCDMA, LTE-FDD	1920	1980	MB
2	GGE, WCDMA, LTE-FDD	1850	1910	MB
3	GGE, WCDMA, LTE-FDD	1710	1785	MB
4	WCDMA, LTE-FDD	1710	1755	MB
5	GGE, WCDMA, LTE-FDD	824	849	LB
6	WCDMA, LTE-FDD	830	840	LB
7	LTE-FDD	2500	2570	HB
8	GGE, WCDMA, LTE-FDD	880	915	LB
9	WCDMA, LTE-FDD	1749.9	1784.9	MB
10	LTE-FDD	1710	1770	MB
11	WCDMA, LTE-FDD	1427.9	1447.9	MB
12	LTE-FDD	699	716	LB
13	LTE-FDD	777	787	LB
14	LTE-FDD	788	798	LB
17	LTE-FDD	704	716	LB
18	WCDMA, LTE-FDD	815	830	LB
19	WCDMA, LTE-FDD	830	845	LB
20	LTE-FDD	832	862	LB
21	LTE-FDD	1447.9	1462.9	MB
23	LTE-FDD	2000	2020	MB
24	LTE-FDD	1626.5	1660.5	MB
25	LTE-FDD	1850	1915	MB
26	LTE-FDD	814	849	LB
27	LTE-FDD	807	824	LB
28	LTE-FDD	703	748	LB
30	LTE-FDD	2305	2315	HB
34	LTE-TDD, TD-SCDMA	2010	2025	MB
38	LTE-TDD	2570	2620	HB
39	LTE-TDD, TD-SCDMA	1880	1920	MB
40	LTE-TDD, TD-SCDMA	2300	2400	HB

BAND	RATs	Lower edge MHz	Upper edge MHz	TX chain
41	LTE-TDD	2496	2690	HB
44	LTE-TDD	703	803	LB
66	LTE-FDD	1710	1780	MB
71	LTE-FDD	663	698	LB
BC6	CDMA2000	1920	1980	MB
BC1/BC14	CDMA2000	1850	1910	MB
B15	CDMA2000	1710	1755	MB
BC0	CDMA2000	815	849	LB
BC4	CDMA2000	1750	1780	MB
BC10	CDMA2000	806	901	LB

Table 5-1. Supported UL frequency bands

5.2 4G FDD/TDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
4G FDD/TDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50Ω load
Output Power Band 1 Band 7 Band 8 Band 40	P_{max}			 0.35 2 1 2	 dBm dBm dBm dBm	1) Pmax: ACLR<Spec 2) Pout (Typ): Pout with Typical front end components 3) Pout Can exceed Pmax in typical conditions
Min Output Power, all bands	P_{min}		-65		dBm	
RF Output Freq. Response HB MB/LB			 1 1		 dB dB	Will be calibrated in RFIC
EUTRA ACLR (Full RB) Band 1 Band 7 Band 8 Band 40			 -43 -43 -43 -43	 -39 -39 -39 -39	 dB dB dB dB	
UTRA1 ACLR (Full RB) Band 1 Band 7 Band 8 Band 40			 -46 -46 -46 -46	 -42 -42 -42 -42	 dB dB dB dB	
EUTRA ACLR (Partial RB) Band 1 Band 7 Band 8 Band 40			 -43 -43 -43 -43	 -39 -39 -39 -39	 dB dB dB dB	
RMS EVM Band 1 Band 7 Band 8 Band 40			 2 2 2 2		 % % % %	 Pout > -14dBm (Post Calibration)
Noise in RX Band 1 Band 2 Band 7 Band 8 Band 13,14			 -158 -157 -158 -157 -154		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	 At Pout = -2.3 dBm At Pout = -2.2 dBm At Pout = -0.9 dBm At Pout = -1.7 dBm At Pout = -1.0 dBm
Additional spurious emission (NS_07 for Flo-3Fbb) Band 13			-68	-65	dBc	Pout = Pmax Spurious measurement RBW = 6.2 kHz Peak search

5.3 3G FDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G FDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Max Output Power Band 1 Band 2 Band 5 Band 8	P_{max}			 1.5 2 1.5 1.5	dBm	 R99 1) Pmax: ACLR<Spec
Min Output Power	P_{min}		-72		dBm	With 12dB digital backoff
Max Output Power (R6 16QAM)	P_{max}			-2	dBm	at B1
Min Output Power (R6 16QAM)	P_{min}		-75		dBm	With 12dB digital backoff
RF Output Frequency Response			0.5	1.0	dB	±2.5MHz offset
ACLR1 (R99) Band 1 Band 2 Band 5 Band 8			 -49 -49 -49 -49	 -45 -45 -45 -45	dBc	 Pout=1.5 dBm Pout=2 dBm Pout=1.5 dBm Pout=1.5 dBm
ACLR2 (R99) Band 1 Band 2 Band 5 Band 8			 -65 -65 -65 -65	 -55 -55 -55 -55	dBc	 Pout=1.5 dBm Pout=2 dBm Pout=1.5 dBm Pout=1.5 dBm
RMS EVM (R99) Band 1 Band 2 Band 5 Band 8			 2.0 2.0 2.0 2.0	 3.5 3.5 3.5 3.5	% 	 Pout=1.5 dBm Pout=2 dBm Pout=1.5 dBm Pout=1.5 dBm
Peak EVM (R99)			8.6		%	Pout= Pmax
RMS EVM (R6 16QAM)			3		%	
Peak EVM (R6 16QAM)			11		%	
Noise Emissions						
Band I, noise in RX			-158		dBc/Hz	Pout= 0 dBm
Band II, noise in RX			-157		dBc/Hz	Pout= 0.5 dBm
Band V, noise in RX			-157		dBc/Hz	Pout= 0 dBm
Band VIII, noise in RX			-157		dBc/Hz	Pout= 0 dBm

5.4 3G TDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G TDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50Ω load
Max Output Power (QPSK) Band 34 Band 39	P_{max}			 2 2	dBm	1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power (QPSK)	P_{min}		-73		dBm	With 12dB digital backoff
Max Output Power (16QAM)	P_{max}			-1	dBm	
Min Output Power (16QAM)	P_{min}		-76		dBm	With 12dB digital backoff
RF Output Frequency Response			0.2		dB	±0.8 MHz offset
ACLR1 (QPSK)			-49	-40	dB	at Pout=2 dBm
ACLR2 (QPSK)			-65	-55	dB	at Pout=2 dBm
RMS EVM (QPSK)			2.0	3.3	%	at Pout=2 dBm
ACLR1 (16QAM)			-49	-40	dB	at Pout=-1 dBm
ACLR2 (16QAM)			-65	-55	dB	at Pout=-1 dBm
RMS EVM (16QAM)			2.0	3.3	%	at Pout=-1 dBm

5.5 3G C2K Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G C2K Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 Ωload
Max Output Power, LB BC0 (Band 5)	P_{out}			0	dBm	1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Max Output Power, MB BC1 (Band 2) BC6 (Band 1) BC15 (Band 4)	P_{out}			 -1.2 -0.5 -1.1	 dBm dBm dBm	1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power	P_{min}		-78		dBm	With 12dB digital backoff
RF Output Frequency Response	P		0.2		dB	±0.6 MHz offset
SEM (1XRTT) at |Δf|:1.25~1.98MHz in 30kHz BW at |Δf|:1.98~4MHz in 30kHz BW			 -59 -66	 -52 -63	 dBc dBc	
SEM (EVDO) at |Δf|:1.25~1.98MHz in 30kHz BW at |Δf|:1.98~4MHz in 30kHz BW			 -56 -66	 -51 -63	 dBc dBc	
RMS EVM			3.5		%	Post calibration
Peak EVM			8.6		%	Post calibration
Carrier suppression				-39	dB	At Pmax, calibrated
Noise Emissions						
BC0, noise in RX			-157		dBc/Hz	
BC1, noise in RX			-157		dBc/Hz	
BC6, noise in RX			-158		dBc/Hz	
BC15, noise in RX			-157		dBc/Hz	

5.6 2G Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
2G Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50Ω load
Max Output Power, LB (GMSK)	P_{max}	1	3	5	dBm	
Max Output Power, HB (GMSK)	P_{max}	1	3	5	dBm	
Max Output Power, LB (8PSK)	P_{max}	-6		0	dBm	1) Pmax: ORFS<Spec 2) Pout can exceed Pmax in typical conditions
Max Output Power, HB (8PSK)	P_{max}	-6		0	dBm	1) Pmax: ORFS<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power, LB (8PSK)	P_{min}			-33	dBm	
Min Output Power, HB (8PSK)	P_{min}			-40	dBm	
ORFS 400k, LB (GMSK)	$ORFS_{400k}$		-66	-64	dBc	
ORFS 400k, HB (GMSK)	$ORFS_{400k}$		-66	-62	dBc	
ORFS 400k, LB (8PSK)	$ORFS_{400k}$		-65	-61	dBc	
ORFS 400k, HB (8PSK)	$ORFS_{400k}$		-64	-60	dBc	
Modulation accuracy (GMSK)						
RMS phase error, LB	RMS		0.8		deg	
RMS phase error, HB	RMS		1.0		deg	
PEAK phase error, LB	Peak		1.5		deg	
PEAK phase error, HB	Peak		2.0		deg	
Modulation accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		1.5		%	
RMS EVM, HB	EVM_{RMS}		2.0		%	
Peak EVM, LB	EVM_{Pk}		5		%	
Peak EVM, HB	EVM_{Pk}		6		%	
Origin offset	OOS		40		dB	
Noise Emissions (GMSK)						

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
20MHz offset, LB			-165	-163	dBc/Hz	
32MHz offset, LB			-166	-164	dBc/Hz	
20MHz offset, HB			-158	-156	dBc/Hz	
32MHz offset, HB			-159	-157	dBc/Hz	
Noise Emissions (8PSK)						
20MHz offset, LB			-160	-158	dBc/Hz	
32MHz offset, LB			-161	-159	dBc/Hz	
20MHz offset, HB			-154	-152	dBc/Hz	
32MHz offset, HB			-155	-153	dBc/Hz	

5.7 Transmitter Power Control Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Power Detector						
RF Input Frequency	F_{det}	663		2690	MHz	
Input Return Loss	S_{11}		-10		dB	Ref. impedance 50Ω
Maximum Input Signal	$P_{det,max}$			0	dBm	
Minimum Input Signal	$P_{det,min}$	-40			dBm	
Measurement Accuracy					dB	
Measurement Time					us	

5.8 Harmonic Suppression

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
All Transmitter Outputs						
Harmonic Emissions						
2nd harmonic						
Band 1			-50		dBc	
Band 7			-50		dBc	
Band 5			-50		dBc	
Band 11			-50		dBc	
Band 13			-50		dBc	
Band 12 (Non HRM)			-50		dBc	
Band 38			-50		dBc	
3rd harmonic						
Band 1			-18		dBc	
Band 7			-18		dBc	
Band 5			-18		dBc	
Band 11			-18		dBc	
Band 13			-50		dBc	
Band 12 (Non HRM)			-18		dBc	
Band 38			-18		dBc	
4th harmonic						
Band 1			-50		dBc	
Band 7			-50		dBc	
Band 5			-50		dBc	
Band 11			-50		dBc	
Band 13			-50		dBc	
Band 12 (Non HRM)			-50		dBc	
Band 38			-50		dBc	

6 Receiver

The direct conversion/LIF receiver (RX) contains all active circuits for the complete receiver chain supporting LTE (TDD/FDD), single-carrier (SC)/dual-carrier (DC) 3G WCDMA, 3G TDSCDMA, C2K and 2G GSM/GPRS/EDGE (GGE) modes reception. The path contains a total of 10+10 single-ended input ports and 1+1 sets of I/Q outputs. Two SAWless Rx input ports PRX 9/10 support for GGE (B2, B3, B5, and B8), TDSCDMA and TDD LTE (B34 and B39). TLFs are designed in SAWless ports to reject out-band blockers. Besides when blocker detectors (BD) detect large blocker, a flag will rise and gain will be adjusted.

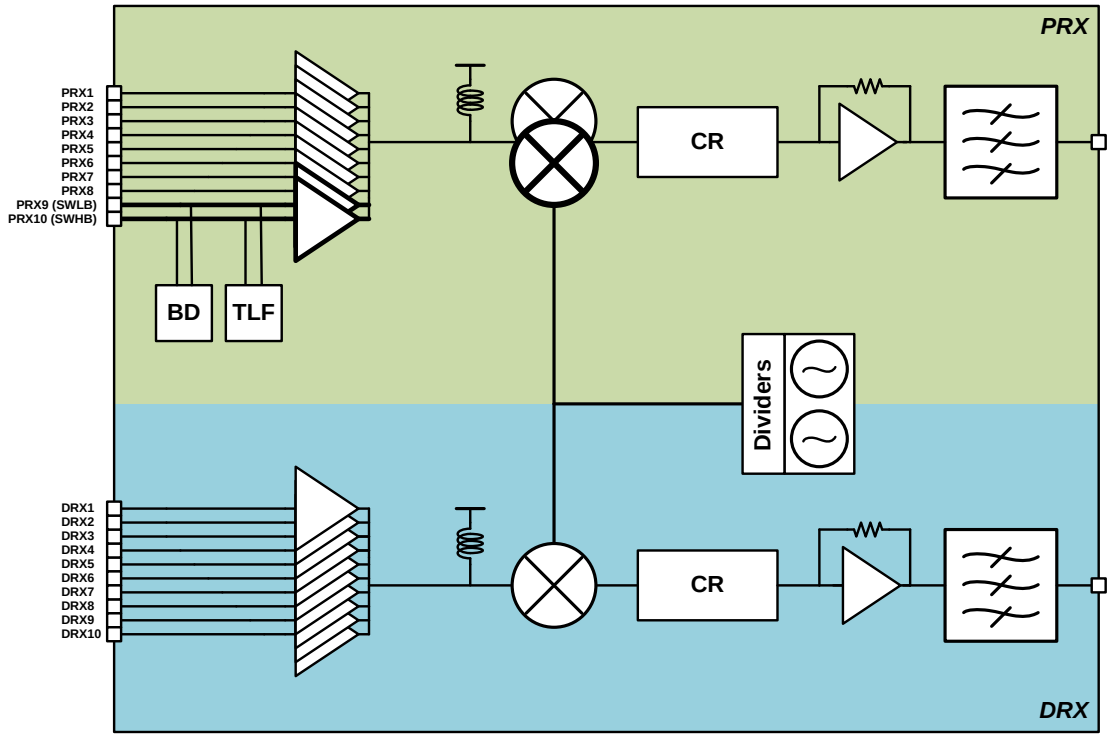


Figure 6-1. Rx block diagram

The analog baseband filter is a low pass filter with programmable transfer function and gain controls. Besides, it contains an RC-calibration circuit, and a DC offset cancellation circuit (DCOC). The low-pass filter is configured as a 2nd-order Butterworth filter for LTE 1.4/3/5/10/15/20/30/40MHz BW, 3G FDD SC, 3G TDD, C2K and GGE modes. Receiver power ON/OFF sequence, LNA/band selection, total receiver gain including LNA, mixer and analog baseband and DCOC timing are controlled by digital circuits.

In addition, IQ calibration is done by injecting an offset frequency test tone generated by the test tone generator (TTG) into the RX mixer. The timing and control of this calibration scheme are also controlled by L1 software and digital circuitry.

Receiver IP2 calibration is done by digital added algorithm to get the optimal receiver parameters in either factory, power-on, or pre-burst. This allows the transceiver to go with low cost front-end components.

The detailed receiver performance is summarized as followings.

6.1 TDSCDMA Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	1880		2400	MHz
Voltage Gain	Max gain: LNA G6; TIA: 63.5dB; Filter: 15dB, Differential output. Note 2		53.6		dB
	Min gain: LNA G1; TIA: 57.5dB; Filter: 0dB, Differential output. Note 2		2.6		dB
LNA Gain Step	LNA High ←→ Mid gain; source VSWR < 1.2		12		dB
	LNA Mid ←→ Low gain; source VSWR < 1.2		18		dB
3 dB Cut-Off Frequency	SC mode. Note 3		1		MHz
Noise Figure	Notes 1, 4; max gain.		2.5	3.5	dB
Input IP3	±3.2MHz and ±6MHz offset. LNA G6, TIA HG, Filter gain=15dB, -38dBm per tone	-12.5	-9.5		dBm
Input IP2	WiFi, max gain; (exclude external devices)	50			dBm
	±4.8MHz and ±4.9MHz LNA G6, TIA HG, Filter gain=15dB, -38dBm per tone	30	35		dBm

6.2 GGE Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	869		1990	MHz
Voltage Gain	Max gain: LNA G6; TIA: 63.5dB; Filter: 15dB, Differential output. Note 2		53.6		dB

Parameter	Conditions	Min.	Nom.	Max.	Unit
	Min gain: LNA G1; TIA: 57.5dB; Filter: 0dB, Differential output. Note 2		2.6		dB
LNA Gain Step	LNA High ←→ Mid gain; source VSWR < 1.2		6		dB
	LNA Mid ←→ Low gain; source VSWR < 1.2		24		dB
3 dB Cut-Off Frequency	Note 3		1		MHz
Noise Figure	Notes 1, 4; max gain; high band		2.5	3.5	dB
	Notes 1, 4; max gain; low band		2.5	3.5	dB
IIP3	±0.8MHz and ±1.6MHz offset; LNA G6, TIA HG, Filter gain=9dB, -42dBm per tone	-15	-13		dBm
IIP2	WiFi, max gain; (exclude external devices)	50			dBm
	±5.94MHz and ±6.06MHz offset; LNA G6, TIA MG, Filter gain=9dB, -27dBm per tone	30	35		dBm

6.3 CDMA2000 Specification

Parameter	Conditions	Min	Nom	Max	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	851		2170	MHz
Max. Voltage Gain	Max gain: LNA G6; TIA: 63.5dB; Filter: 15dB, Differential output. Note 2		53.6		dB
Min. Voltage Gain	Min gain: LNA G1; TIA: 63.5dB; Filter: 0dB, Differential output. Note 2		8.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB
	LNA G2 ←→ G1		6		dB
TIA Gain Step	Fixed TIA at HG				
LPF Gain Step	Range from 0dB to 15dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	Note 2		1		MHz
Test condition 1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;			2.5	3.5	dB
IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
IIP2	At TX offset		55		dBm

Parameter	Conditions	Min	Nom	Max	Unit
Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Test condition 2 (LNA=G5, TIA=HG, LPF=3dB) [ACS1]					
Noise Figure Notes 1, 3;			7		dB
IIP3	LNA=G5, TIA=HG, LPF=3dB		-5		dBm
Voltage Gain	LNA=G5, TIA=HG, LPF=3dB		35.6		dB
Test condition 3 (LNA=G5, TIA=HG, LPF=6dB) [STD]					
Noise Figure Notes 1, 3;			7		dB
IIP3	LNA=G5, TIA=HG, LPF=6dB		-7		dBm
Voltage Gain	LNA=G5, TIA=HG, LPF=6dB		38.6		dB

6.4 WCDMA Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	869		2170	MHz
Max. Voltage Gain	Max gain: LNA G6; TIA: 63.5dB; Filter: 15dB, Differential output. Note 2		53.6		dB
Min. Voltage Gain	Min gain: LNA G1; TIA: 63.5dB; Filter: 0dB, Differential output. Note 2		8.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB
	LNA G2 ←→ G1		6		dB
TIA Gain Step	Fixed TIA at HG				
LPF Gain Step	Range from 0dB to 15dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	BW=5MHz mode. Note 2		3		MHz
Test condition 1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;			2.5	3.5	dB
IIP3	LNA=G6, TIA=HG, LPF=12dB		-7		dBm

Parameter	Conditions	Min.	Nom.	Max.	Unit
IIP2	At TX offset		55		dBm
Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Test condition 2 (LNA=G6, TIA=HG, LPF=9dB) [ACS1]					
Noise Figure Notes 1, 3;			6		dB
IIP3	LNA=G6, TIA=HG, LPF=9dB		-7		dBm
Voltage Gain	LNA G6; TIA HG and LPF=9dB.		47.6		dB
Test condition 3 (LNA=G4, TIA=HG, LPF=6dB) [NBB]					
Noise Figure Notes 1, 3;			11		dB
IIP3	LNA=G4, TIA=HG, LPF=6dB		-5		dBm
Voltage Gain	LNA= G4; TIA =HG and LPF=6dB.		32.6		dB
Test condition 4 (LNA=G1, TIA=HG, LPF=3dB) [ACS2]					
Noise Figure Notes 1, 3;			33		dB
IIP3	LNA=G1, TIA=HG, LPF=3dB		7		dBm
Voltage Gain	LNA=G1, TIA=HG, LPF=3dB		11.6		dB
Test condition 5 (LNA=G1, TIA=HG, LPF=-3dB) [Maximum Input]					
Noise Figure Notes 1, 3;			36		dB
Voltage Gain	LNA=G1, TIA=HG, LPF=0dB		8.6		dB

6.5 LTE Specification

- Non/inter-band/intra-band contiguous CA scenario

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	617		2700	MHz
Max. Voltage Gain	Max gain: LNA G6; TIA: 63.5dB; Filter: 15dB, Differential output. Note 2		53.6		dB
Min. Voltage Gain	Min gain: LNA G1; TIA: 63.5dB; Filter: 0dB, Differential output. Note 2		8.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB

Parameter	Conditions	Min.	Nom.	Max.	Unit
	LNA G2 ←→ G1		6		dB
TIA Gain Step	TIA HG ←→ MG		6		dB
	TIA MG ←→ LG		6		dB
LPF Gain Step	Range from 0dB to 15dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	BW=1.4MHz mode. Note 2		1		MHz
	BW=3MHz mode. Note 2		3		MHz
	BW=5MHz mode. Note 2		3		MHz
	BW=10MHz mode. Note 2		5		MHz
	BW=15MHz mode. Note 2		7.5		MHz
	BW=20MHz mode. Note 2		10		MHz
	BW=30MHz mode. Note 2		15.7		MHz
	BW=40MHz mode. Note 2		20.8		MHz
Test condition 1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		2.5	3.5	dB
	2300MHz < frequency <2700MHz		2.6	3.6	dB
IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
IIP2	At TX offset		55		dBm
Voltage Gain	LNA=G6, TIA=HG, LPF=15dB		53.6		dB
Test condition 2 (LNA=G5, TIA=HG, LPF=3dB) [ACS1]					
Noise Figure Notes 1, 3;			7		dB
IIP3	LNA=G5, TIA=HG, LPF=3dB		-5		dBm
Voltage Gain	LNA=G5, TIA=HG, LPF=3dB		35.6		dB
Test condition 3 (LNA=G4, TIA=HG, LPF=6dB) [NBB]					
Noise Figure Notes 1, 3;			13.5		dB
IIP3	LNA=G4, TIA=HG, LPF=6dB		0		dBm
Voltage Gain	LNA=G4, TIA=HG, LPF=6dB		32.6		dB
Test condition 4 (LNA=G2, TIA=HG, LPF=0dB) [ACS2]					
Noise Figure Notes 1, 3;			25.2		dB
IIP3	LNA=G2, TIA=HG, LPF=0dB		7		dBm
Voltage Gain	LNA=G2, TIA=HG, LPF=0dB		14.6		dB
Test condition 5 (LNA=G1, TIA=HG, LPF=-6dB) [Maximum Input]					

Parameter	Conditions	Min.	Nom.	Max.	Unit
Noise Figure Notes 1, 3;			36		dB
Voltage Gain	LNA=G1, TIA=HG, LPF=0dB		8.6		dB

Note 1: Source/Reference impedance: 50 Ω
Note 2: After RC calibration
Note 3: No blockers.
Note 4: Includes RX LDO, LNA/MXR, SRX and LO path, TIA, and RXABB

7 Digital Control Interfaces

7.1 Introduction

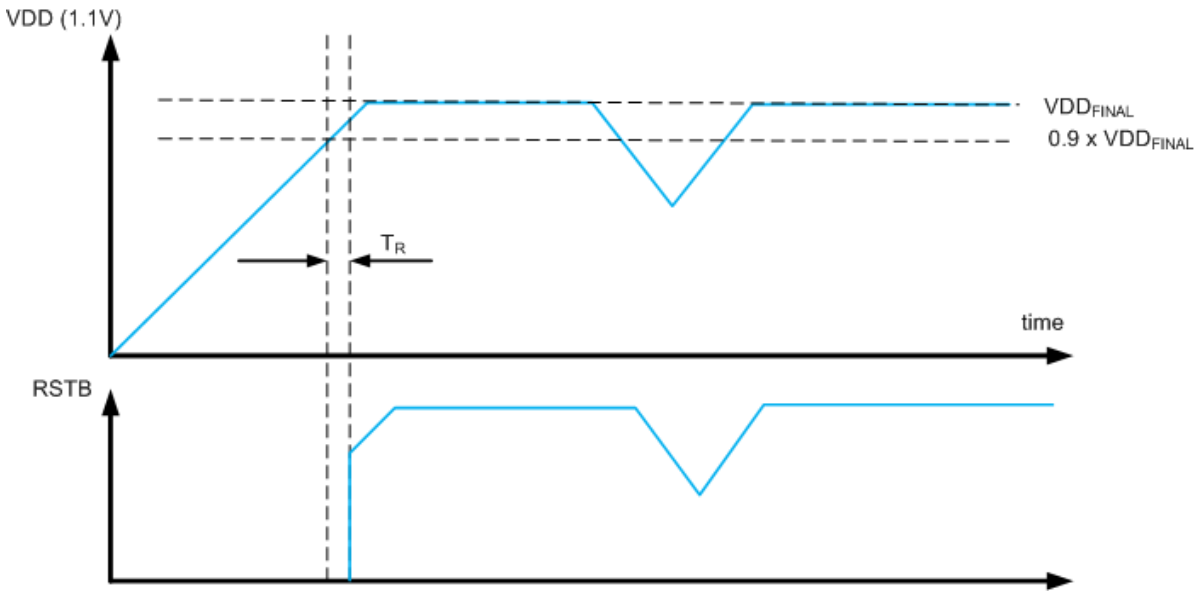
RFSYS is programmed through five BSI GPIO PADs. Both write and read operations are supported and five wires are used (three bi-direction data pins, one clock pin, and one enable pin). All BSI interfaces are through VIO18 domain.

7.2 Power-on Reset

The chip includes a Power-On Reset (POR) operating from the static domain LDO's on the VIO18 domain. This GLOBAL_STATIC digital blocks operates from the 1.1V supply domain directly derived from VIO18 via LDO's. The important point then is that the reset needs to be active for sufficiently long that the power supply has stabilized but short enough that the domain is available for BSI programming when requested.

In the case of the GS LDO VIO18 is always present (in normal mode) and the LDO for this domain is enabled from the baseband.

The operation is shown in the figure below.



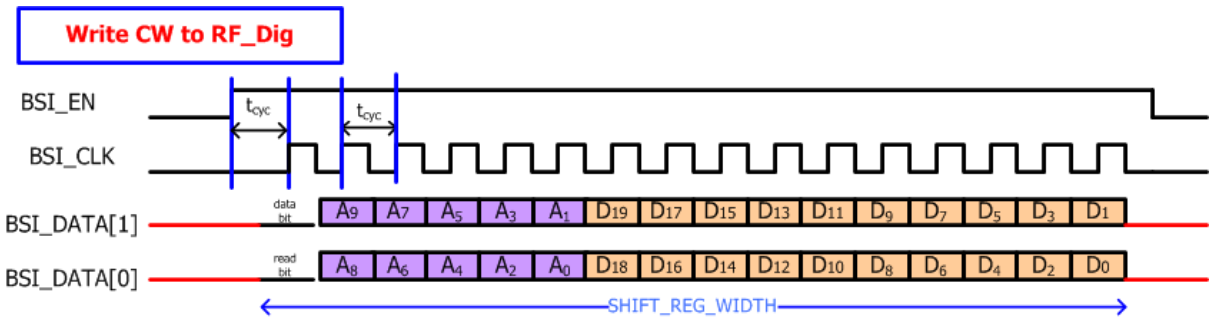
Parameter	Conditions	Min	Nom	Max	Unit	Notes
Reset Active Time T_R	Over range of full VIO18 ramp times	5		200	µs	
VDD		0.8	1.1	1.25	V	
Trigger Point V_{TH}			0.9 x VDD		V	
Idd Quiescent current				<100	nA	

7.3 BSI Interface

The BSI Clock is designed to operate at a maximum frequency of 68.25 MHz (1092/8/2), switching down to 34.125(68.25/2) or 22.75 (8.25/3)MHz during the read back phase of a read operation.

The BSI clock has nominally a 50% duty cycle (< 40:60 should be guaranteed by the baseband clock generator). The following figure shows the timing diagram of write and read operations via BSI interface.

BSI write waveform:



BSI read waveform: